# SIMPLE SWITCHER 3.8V - 36V、3A
# 同步降压转换器

## 特性

- 输入电压范围：3.8V 至 36V
- 输出电压范围：1V 至 24V
- 输出电流：3A
- 75mΩ/50mΩ $R_{DS-ON}$ 功率 MOSFET
- 峰值电流模式控制
- 最短导通时间很短，只有 68ns
- 频率：450kHz、1.4MHz、2.1MHz
- 结温范围为 –40°C 至 +125°C
- 低 EMI 和低开关噪声
- 集成补偿网络
- 低 EMI 和开关噪声
- 可在所有负载下进行高效电源转换
  - 峰值效率 > 95%
  - 低至 25μA 的工作静态电流

## 概述

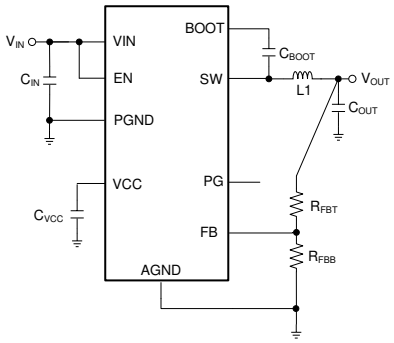
SR33630 SIMPLE SWITCHER 稳压器是一款简单易用的同步降压直流/直流转换器，可提供出色的效率，适用于条件严苛的工业应用。SR33630 能够使用高达 36V 的输入电压驱动高达 3A 的负载电流，还以超小的解决方案尺寸提供出色的轻负载效率和输出精度。电源正常状态标志和精密使能端等特性有助于实现灵活而又易用的解决方案，适用于广泛的应用。SR33630 在轻负载条件下自动折返频率以提高效率。此器件通过集成技术省去了大部分外部元件，并提供专为实现简单 PCB 布局而设计的引脚排列方式。保护特性包括热关断、输入欠压锁定、逐周期电流限制和断续短路保护。SR33630 采用 8 引脚 HSOIC 封装和具有可湿性侧面的 12 引脚 3mm × 2mm 新一代 VQFN 封装。该器件还具有符合 AEC-Q100 标准的版本。

器件信息

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| SR33630ADDA | HSOIC-8P | 5.00mm × 4.00mm |
| SR33630ARNX | VQFN-12P | 3.00mm × 2.00mm |

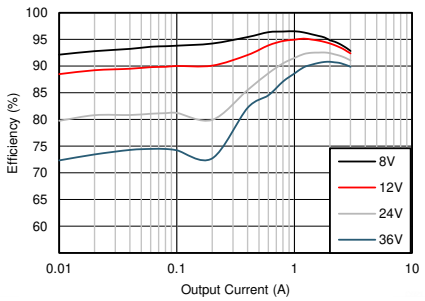
## 应用领域

- 电机驱动系统：无人机、交流逆变器、变频驱动器、伺服系统
- 工厂和楼宇自动化系统：PLC CPU、HVAC 控制、电梯控制
- 通用宽输入电压电源



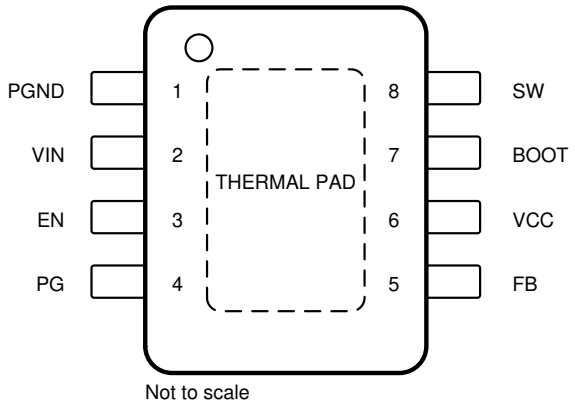

典型应用电路

效率与输出电流间的关系

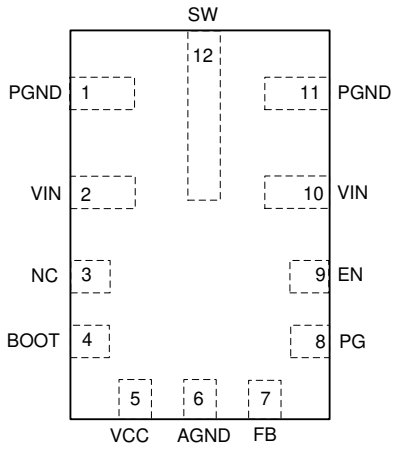



$V_{OUT}$ = 5V，450kHz，VQFN

## Pin Configuration and Functions / 引脚定义与功能描述




**HSOIC-8P**
**(Top View)**




**VQFN-12P**
**(Top View)**

### Pin Functions

| PIN | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| HSOIC | VQFN | NAME | | |
| 1 | 1,11 | PGND | G | Power ground terminal. Connect to system ground and AGND. Connect to bypass capacitor with short wide traces. |
| 2 | 2,10 | VIN | P | Input supply to regulator. Connect a high-quality bypass capacitor or capacitors directly to this pin and PGND. |
| 3 | 9 | EN | A | Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; *Do not float*. |
| 4 | 8 | PG | A | Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Flag pulls low when EN = Low. Can be left open when not used. |
| 5 | 7 | FB | A | Feedback input to regulator. Connect to tap point of feedback voltage divider. *Do not float. Do not ground*. |
| 6 | 5 | VCC | P | Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND. |
| 7 | 4 | BOOT | P | Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the $C_{BOOT}$ capacitor to the SW pin. |
| 8 | 12 | SW | P | Regulator switch node. Connect to power inductor. On the VQFN package connect the SW pin to NC on the PCB. This simplifies the connection from the $C_{BOOT}$ capacitor to the SW pin. |
| THERMAL PAD | 6 | AGND | G | Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB. For the HSOIC package, the pad on the bottom of the device serves as both the AGND connection and a thermal connection to the heat sink ground plane. This pad must be soldered to a ground plane to achieve good electrical and thermal performance. |
| — | 3 | NC | — | On the VQFN package the SW pin must be connected to NC on the PCB. This simplifies the connection from the $C_{BOOT}$ capacitor to the SW pin. This pin has no internal connection to the regulator. |
| A = Analog, P = Power, G = Ground | | | | |

# Specifications /技术参数

## Absolute Maximum Ratings / 极限参数

Over the recommended operating junction temperature range

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltages | VIN to PGND | -0.3 | 38 | V |
| | EN to AGND | -0.3 | $V_{IN}$ + 0.3 | |
| | FB to AGND | -0.3 | 5.5 | |
| | PG to AGND | 0 | 22 | |
| | AGND to PGND | -0.3 | 0.3 | |
| | SW to PGND | -0.3 | $V_{IN}$ + 0.3 | V |
| | SW to PGND less than 100-ns transients | -3.5 | 38 | |
| | BOOT to SW | -0.3 | 5.5 | |
| | VCC to AGND | -0.3 | 5.5 | |
| $T_J$ | Junction temperature | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature | -55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V
(3) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.
(4) Under some operating conditions the VCC LDO voltage may increase beyond 5.5V.

## ESD Ratings / 静电放电参数

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM) | ±2500 | V |
| | | Charged-device model (CDM) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions / 推荐操作条件

Over the recommended operating temperature range of -40 °C to 125 °C (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN to PGND | 3.8 | 36 | V |
| | EN | 0 | $V_{IN}$ | |
| | PG | 0 | 18 | |
| Adjustable output voltage | $V_{OUT}$ | 1 | 24 | V |
| Output current | $I_{OUT}$ | 0 | 3 | A |

## Thermal Information / 热性能信息

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

| THERMAL METRIC | | SR33630 | | UNIT |
|---|---|---|---|---|
| | | DDA (HSOIC) | RNX (VQFN) | |
| | | 8 PINS | 12 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 42.9 | 72.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 54 | 35.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.6 | 23.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 4.3 | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.8 | 23.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.3 | N/A | °C/W |

## Electrical Characteristics /电气特性

Limits apply over the operating junction temperature ($T_J$) range of －40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN}$ = 12 V, $V_{EN}$ = 4 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| $V_{IN}$ | Minimum operating input voltage | | | | 3.8 | V |
| $I_Q$ | Non-switching input current; measured at VIN pin | $V_{FB}$ = 1.2 V | | 24 | 34 | μA |
| $I_{SD}$ | Shutdown quiescent current; measured at VIN pin | EN = 0 | | 5 | 10 | μA |
| **ENABLE** | | | | | | |
| $V_{EN-VCC-H}$ | EN input level required to turn on internal LDO | Rising threshold | | | 1 | V |
| $V_{EN-VCC-L}$ | EN input level required to turn off internal LDO | Falling threshold | 0.3 | | | V |
| $V_{EN-H}$ | EN input level required to start switching | Rising threshold | 1.2 | 1.231 | 1.26 | V |
| $V_{EN-HYS}$ | Hysteresis below $V_{EN-H}$ | Hysteresis below $V_{EN-H}$; falling | | 100 | | mV |
| $I_{LKG-EN}$ | Enable input leakage current | $V_{EN}$ = 3.3 V | | 0.2 | | nA |
| **INTERNAL SUPPLIES** | | | | | | |
| VCC | Internal LDO output voltage appearing at the VCC pin | 6 V ≤ $V_{IN}$ ≤ 36 V | 4.75 | 5 | 5.25 | V |
| $V_{BOOT-UVLO}$ | Bootstrap voltage undervoltage lock-out threshold | | | 2.2 | | V |
| **VOLTAGE REFERENCE (FB PIN)** | | | | | | |
| $V_{FB}$ | Feedback voltage; ADJ option | | 0.985 | 1 | 1.015 | V |
| $I_{FB}$ | Current into FB pin; ADJ option | FB = 1 V | | 0.2 | 50 | nA |
| **CURRENT LIMITS** | | | | | | |
| $I_{SC}$ | High-side current limit | SR33630 | 3.85 | 4.5 | 5.05 | A |
| $I_{LIMIT}$ | Low-side current limit | SR33630 | 2.9 | 3.5 | 4.1 | A |
| $I_{PEAK-MIN}$ | Minimum peak inductor current | SR33630 | | 0.69 | | A |

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| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{ZC}$ | Zero current detector threshold | | | -0.106 | | A |
| **SOFT START** | | | | | | |
| $t_{SS}$ | Internal soft-start time | | 2.9 | 4 | 6 | ms |
| **POWER GOOD (PG PIN)** | | | | | | |
| $V_{PG-HIGH-UP}$ | Power-good upper threshold - rising | % of FB voltage | 105% | 107% | 110% | |
| $V_{PG-HIGH-DN}$ | Power-good upper threshold - falling | % of FB voltage | 103% | 105% | 108% | |
| $V_{PG-LOW-UP}$ | Power-good lower threshold - rising | % of FB voltage | 92% | 94% | 97% | |
| $V_{PG-LOW-DN}$ | Power-good lower threshold - falling | % of FB voltage | 90% | 92% | 95% | |
| $t_{PG}$ | Power-good glitch filter delay | | 60 | | 170 | μs |
| $R_{PG}$ | Power-good flag $R_{DSON}$ | $V_{IN}$ = 12 V, $V_{EN}$ = 4 V | | 76 | 150 | Ω |
| | | $V_{EN}$ = 0 V | | 35 | 60 | |
| $V_{IN-PG}$ | Minimum input voltage for proper PG function | 50-μA, EN = 0 V | | | 2 | V |
| $V_{PG}$ | PG logic low output | 50-μA, EN = 0 V, $V_{IN}$ = 2V | | | 0.2 | V |
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Switching frequency | "A" Version | 340 | 450 | 460 | kHz |
| $f_{SW}$ | Switching frequency | "B" Version | 1.2 | 1.4 | 1.6 | MHz |
| $f_{SW}$ | Switching frequency | "C" Version, DDA package | 1.8 | 2.1 | 2.4 | MHz |
| $f_{SW}$ | Switching frequency | "C" Version, RNX package | 1.8 | 2.1 | 2.3 | MHz |
| **MOSFETS** | | | | | | |
| $R_{DS-ON-HS}$ | High-side MOSFET ON-resistance | RNX package | | 75 | 145 | mΩ |
| $R_{DS-ON-HS}$ | High-side MOSFET ON-resistance | DDA package | | 95 | 160 | mΩ |
| $R_{DS-ON-LS}$ | Low-side MOSFET ON-resistance | RNX package | | 50 | 95 | mΩ |
| $R_{DS-ON-LS}$ | Low-side MOSFET ON-resistance | DDA package | | 66 | 110 | mΩ |

(1) See *Power-Good Flag Output* for details.
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) When the voltage across the $C_{BOOT}$ capacitor falls below this voltage, the low side MOSFET is turned on to recharge $C_{BOOT}$.
(4) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

## Timing Requirements / 时间需求

Limits apply over the operating junction temperature ($T_J$) range of －40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J$ = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: $V_{IN}$ = 12 V, $V_{EN}$ = 4 V.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ON-MIN}$ | Minimum switch on-time | RNX package | | 68 | 80 | ns |
| $t_{ON-MIN}$ | Minimum switch on-time | DDA package | | 75 | 108 | ns |
| $t_{OFF-MIN}$ | Minimum switch off-time | RNX package | | 52 | 70 | ns |
| $t_{OFF-MIN}$ | Minimum switch off-time | DDA package | | 50 | 85 | ns |
| $t_{ON-MAX}$ | Maximum switch on-time | | | 7 | 9 | μs |

## System Characteristics / 系统特性

The following specifications apply to a typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to $T_J$ = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of $T_J$ = －40°C to 125°C. *These specifications are not ensured by production testing.*

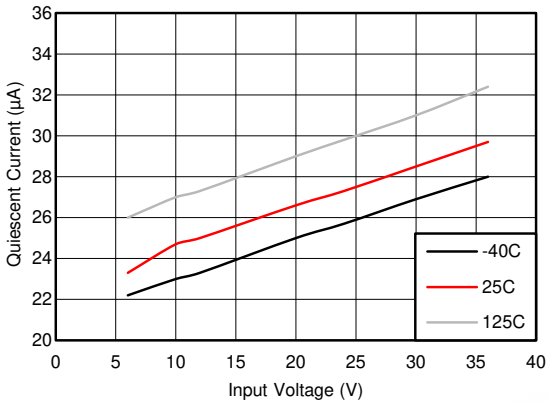
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating input voltage range | $V_{OUT}$ = 3.3 V, $I_{OUT}$= 0 A | 3.8 | | 36 | V |
| $V_{OUT}$ | Output voltage regulation for $V_{OUT}$ = 5 V | $V_{OUT}$ = 5 V, $V_{IN}$ = 7 V to 36 V, $I_{OUT}$ = 0 A to max. load | －1.5% | | 2.5% | |
| | | $V_{OUT}$ = 5 V, $V_{IN}$ = 7 V to 36 V, $I_{OUT}$ = 1 A to max. load | －1.5% | | 1.5% | |
| | Output voltage regulation for $V_{OUT}$ = 3.3 V | $V_{OUT}$ = 3.3 V, $V_{IN}$ = 3.8 V to 36 V, $I_{OUT}$ = 0 A to max. load | －1.5% | | 2.5% | |
| | | $V_{OUT}$ = 3.3 V, $V_{IN}$ = 3.8 V to 36 V, $I_{OUT}$ = 1 A to max. load | －1.5% | | 1.5% | |
| $I_{SUPPLY}$ | Input supply current when in regulation | $V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 0 A, $R_{FBT}$ = 1 MΩ | | 25 | | μA |
| $V_{DROP}$ | Dropout voltage; ($V_{IN}$ － $V_{OUT}$) | $V_{OUT}$ = 5 V, $I_{OUT}$ = 1A Dropout at －1% of regulation, $f_{SW}$ = 140 kHz | | 150 | | mV |
| $D_{MAX}$ | Maximum switch duty cycle | $V_{IN}$ = $V_{OUT}$ = 12 V, $I_{OUT}$ = 1 A | | 98% | | |
| $V_{HC}$ | FB pin voltage required to trip short-circuit hiccup mode | | | 0.4 | | V |
| $t_{HC}$ | Time between current-limit hiccup burst | | | 94 | | ms |
| $t_D$ | Switch voltage dead time | | | 2 | | ns |
| $T_{SD}$ | Thermal shutdown temperature | Shutdown temperature | | 165 | | °C |
| | | Recovery temperature | | 148 | | °C |

(1) Deviation is with respect to $V_{IN}$ =12 V, $I_{OUT}$ = 1 A.

(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: $f_{MIN}$ = 1 / ($t_{ON-MAX}$ + $t_{OFF-MIN}$). $D_{MAX}$ = $t_{ON-MAX}$ /($t_{ON-MAX}$ + $t_{OFF-MIN}$).

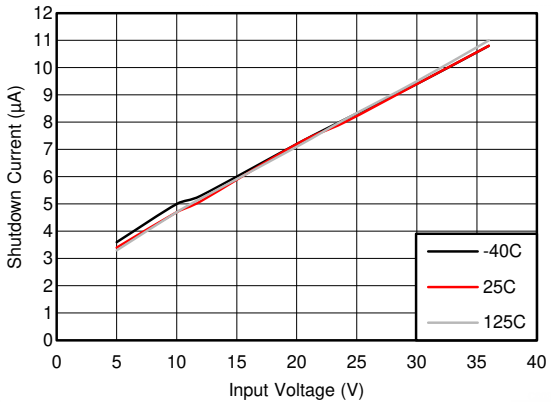
## Typical Characteristics/典型特性

Unless otherwise specified the following conditions apply: $T_A$ = 25°C and $V_{IN}$ = 12 V



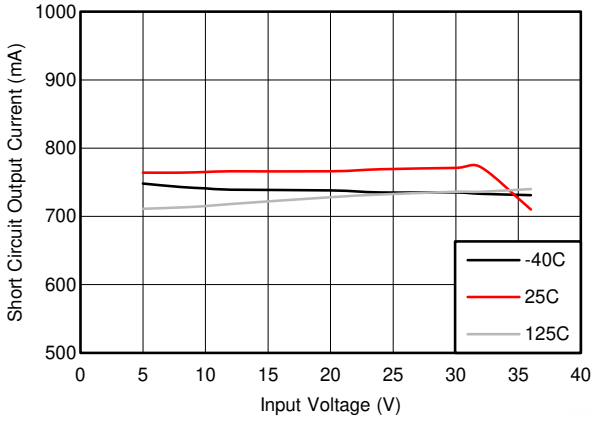

$V_{FB}$ = 1.2 V

**1. Non-Switching Input Supply Current**



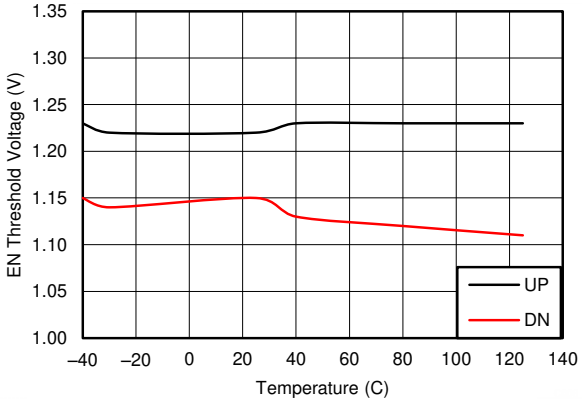

EN = 0 V

**2. Shutdown Supply Current**

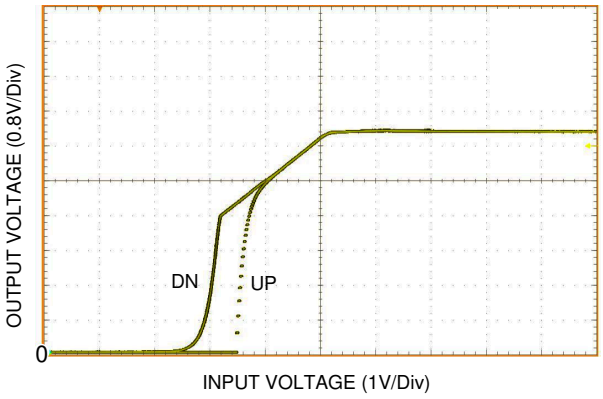



$V_{OUT}$ = 0 V $f_S$ = 450 kHz

**3. Short-Circuit Output Current**

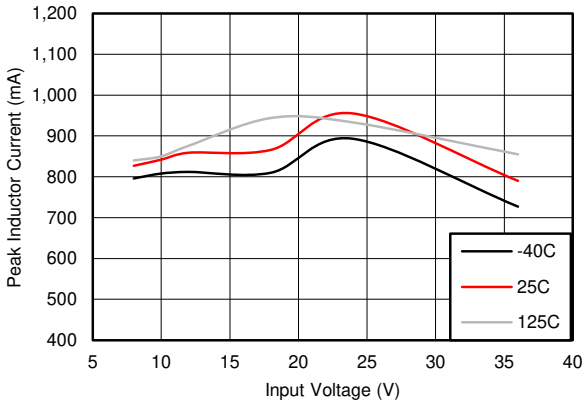



**4. Precision Enable Thresholds**




$I_{OUT}$ = 1 mA

**5. UVLO Thresholds**




$I_{OUT}$ = 0 A $V_{OUT}$ = 5 V $f_{SW}$ = 450 kHz

**6. $I_{PEAK-MIN}$**