

# 36V, 200mA Low Dropout Voltage Linear Regulator

## General Description

The SR8367 series are a group of low-dropout ( LDO ) voltage regulators offering the benefits of wide input voltage range, low dropout voltage, low power consumption, and miniaturized packaging.

Quiescent current of only 2.2 $\mu$ A makes these devices ideal for powering the battery-powered, always-on systems that require very little idle-state power dissipation to a longer service life.

The SR8367 series of linear regulators are stable with the ceramic output capacitor over its wide input range from 2V to 36V and the entire range of output load current (0mA to 200mA).

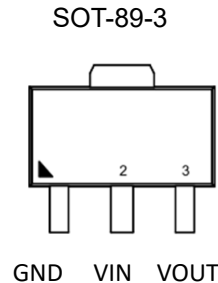
## Features

- 2.2 $\mu$ A Ground Current at no Load
- $\pm 2\%$  Output Accuracy
- 200mA Output Current
- Wide Operating Input Voltage Range: 2V to 36V
- Dropout Voltage: 0.66V at 100mA /  $V_{OUT}$  5V
- Support Fixed Output Voltage 1.8V, 3.3V, 5V, 9V, 12V
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- SOT-89-3 Package Available

## Applications

- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems
- Industrial Controls
- Weighting Scales
- Meters
- Home Automation

## Pin Configurations



## Ordering Information

 SR8367-**AA****BB**

Designator	Description	Symbol	Description
<b>AA</b>	Output Voltage	18	$V_{OUT} = 1.8V$
		..	..
		..	..
		99	$V_{OUT} = 9.9V$
		A1	$V_{OUT} = 12V$
<b>BB</b>	Package type	A3	SOT-89-3

Special Request: Any Voltage between 1.8V and 12V under specific business agreement

## Description of Functional Pins

Pin No	Pin Name	Pin Function
1	GND	Ground
2	VIN	Input of Supply Voltage.
3	VOUT	Output of the Regulator

### Typical Application Circuits

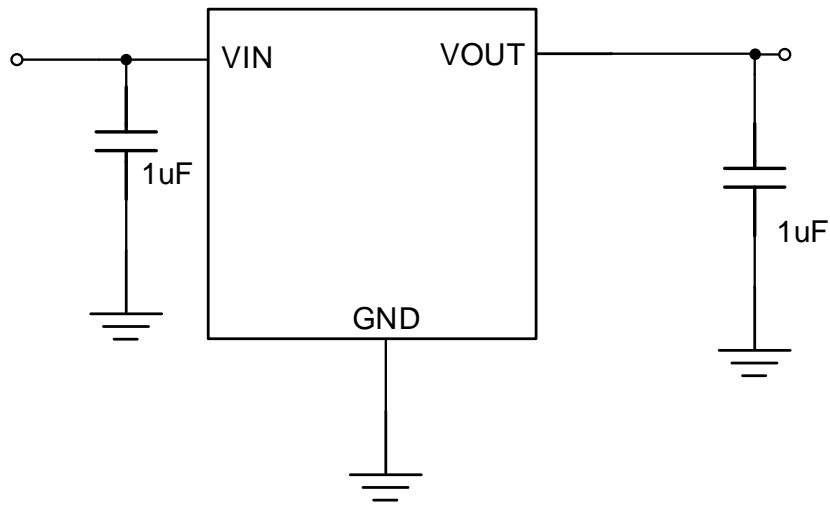
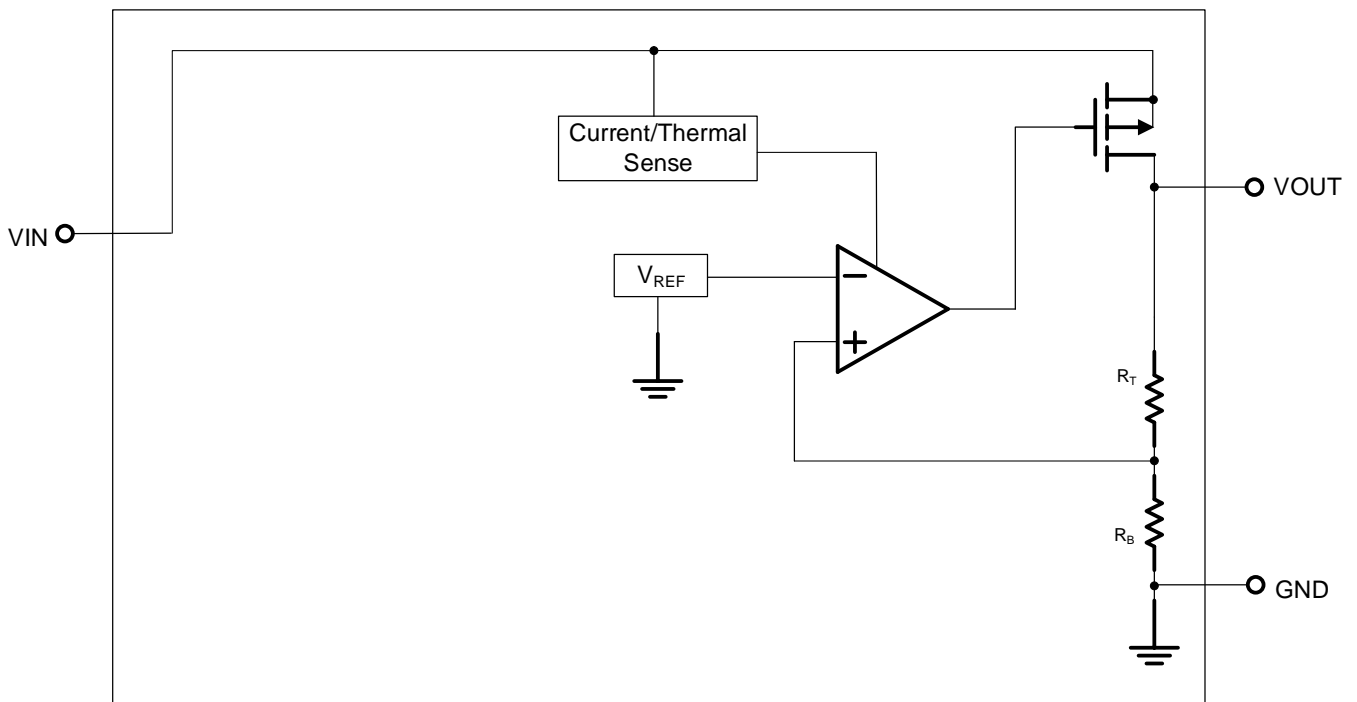


Figure 1: Application circuit of Fixed  $V_{OUT}$  LDO

### Function Block Diagram



**Absolute Maximum Ratings** (Note 1)

VIN to GND -----	-0.3V to 40V
VOUT to GND	
SR8367-A1, SR8367-90 -----	-0.3V to 14V
SR8367-18, SR8367-33, SR8367-50 -----	-0.3V to 6.0V
VOUT to VIN -----	-40V to 0.3V
Package Thermal Resistance (Note 2)	
SOT-89-3, $\theta_{JA}$ -----	120 °C /W
Lead Temperature (Soldering, 10 sec.) -----	260 °C
Junction Temperature -----	150 °C
Storage Temperature Range -----	-60 °C to 150 °C
ESD Susceptibility	
HBM -----	2KV
MM -----	200V

**Recommended Operating Conditions**

Input Voltage VIN -----	2.0V to 36V
Junction Temperature Range -----	-40 °C to 125 °C
Ambient Temperature Range -----	-40 °C to 85 °C

## Electrical Characteristics

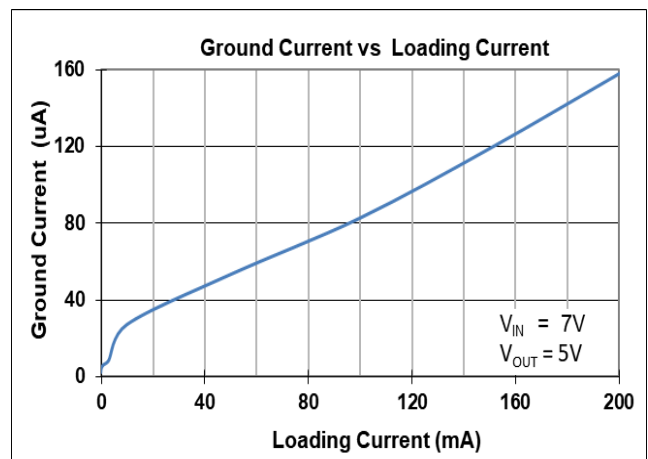
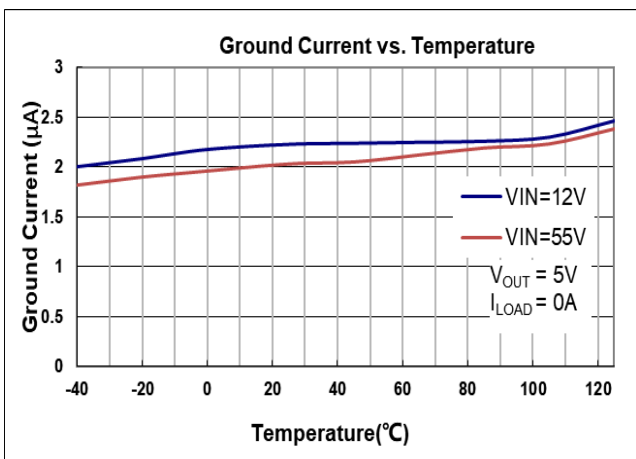
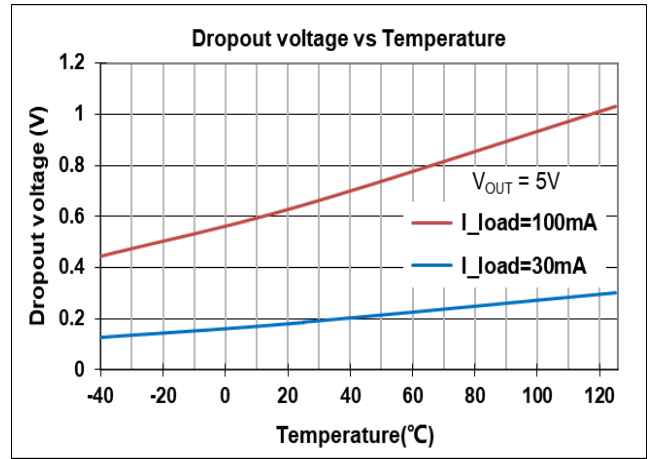
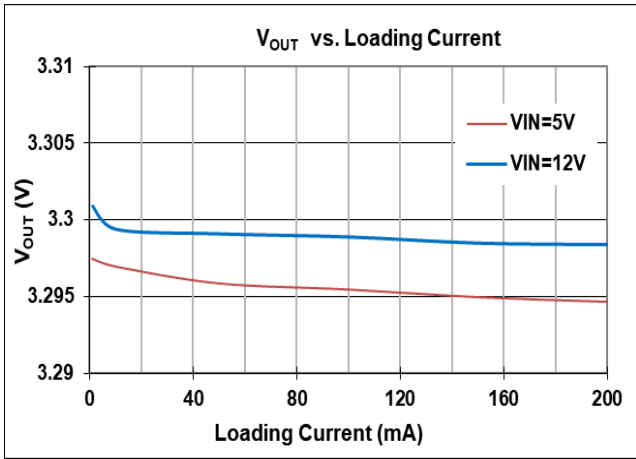
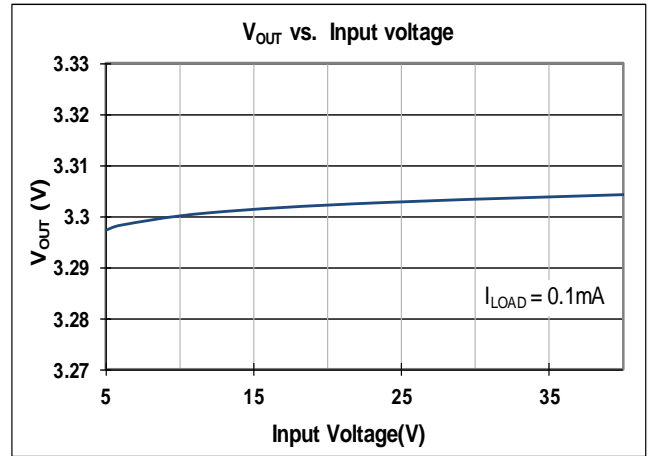
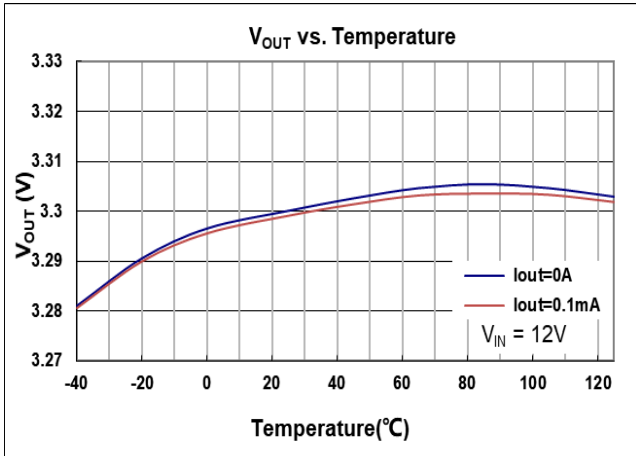
( $V_{IN} = 15V$ ,  $V_{EN} = 5V$ ,  $T_A = 25^\circ C$  unless otherwise specified)

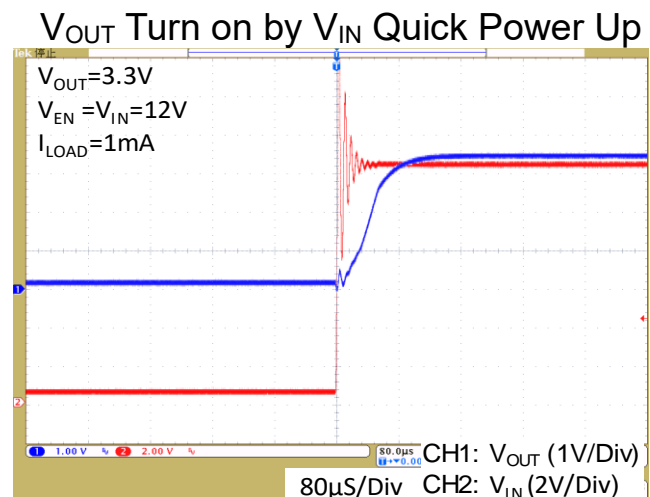
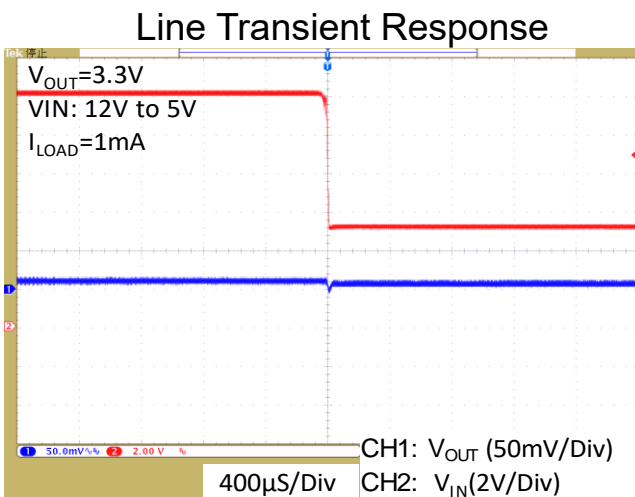
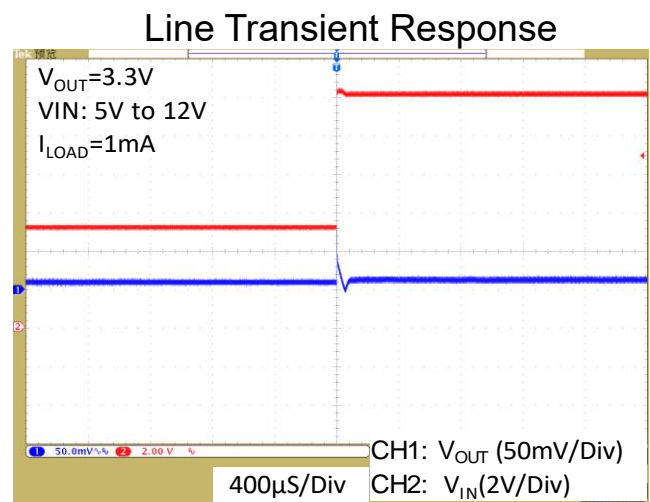
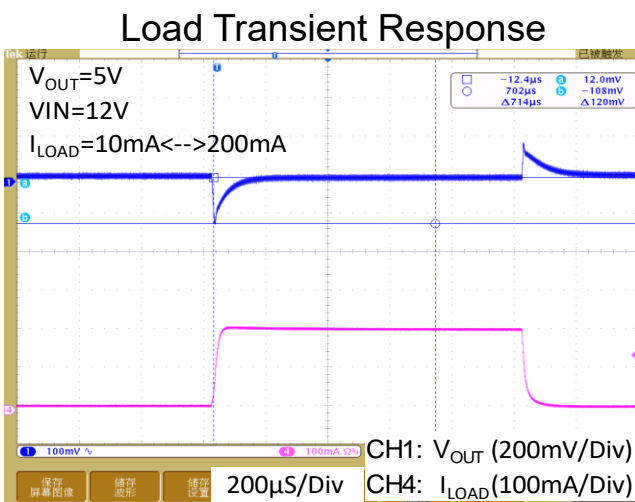
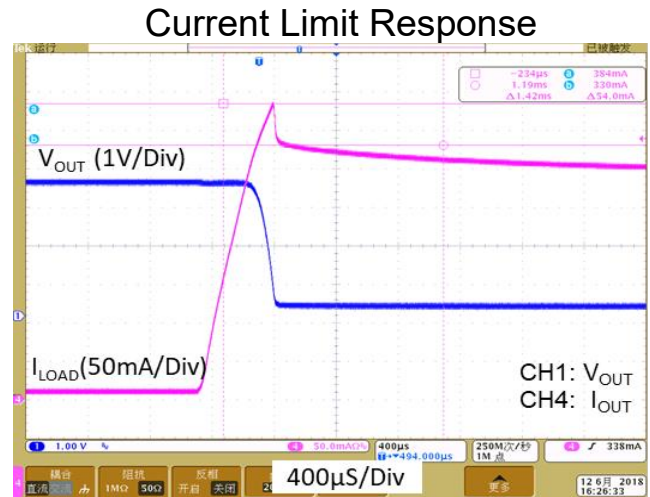
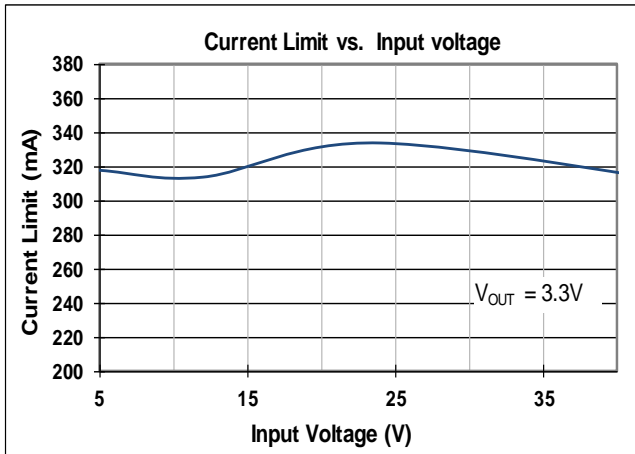
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	$V_{IN}$		2	--	36	V
DC Output Voltage Accuracy		$I_{LOAD} = 0.1mA$	-2		2	%
Dropout Voltage ( $I_{LOAD} = 100mA$ )	$V_{DROP}$	$V_{OUT} \geq 5V$	--	0.66		V
	$V_{DROP\_3.3V}$	$V_{OUT} = 3.3V$		0.75		
	$V_{DROP\_1.8V}$	$V_{OUT} = 1.8V$		1		
Ground Current ( $I_{LOAD} = 0mA$ )	$I_Q$	$V_{OUT} \leq 5V$		2.2		$\mu A$
	$I_{QH}$	$5V < V_{OUT} \leq 12V$		4.2		
Line Regulation	$\Delta LINE$	$I_{LOAD} = 1mA$ , $5 \leq V_{IN} \leq 36V$	--	0.3		%
Load Regulation	$\Delta LOAD$	$1mA \leq I_{LOAD} \leq 0.2A$		0.1		%
Output Current Limit	$I_{LIM}$	$V_{OUT} = 0$	201	300		mA
Power Supply Rejection Ratio	PSRR	$V_{OUT} = 5V$ , $I_{LOAD} = 1mA$ , $V_{IN} = 12V$ , $f = 100Hz$		70		dB
Thermal Shutdown Temperature	$T_{SD}$	$I_{LOAD} = 10mA$	--	160	--	$^\circ C$
Thermal Shutdown Hysteresis	$\Delta T_{SD}$				15	

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^\circ C$  on a DS-Tech EVB board.

Typical Characteristics





## Application Guideline

### ***Input and Output Capacitor Requirements***

The external input and output capacitors of SR8367 series must be properly selected for stability and performance. Use a 1 $\mu$ F or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1m $\Omega$  ESR ( Equivalent Series Resistance ) and effective capacitance between 1 $\mu$ F and 22 $\mu$ F requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

### ***Current Limit***

The SR8367 series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 300mA ( typical ). The output can be shorted to ground indefinitely without damaging the part.

### ***Dropout Voltage***

The SR8367 series use a PMOS pass transistor to achieve low dropout. When ( VIN – VOUT ) is less than the dropout voltage ( V<sub>DROP</sub> ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the RDS(ON) of the PMOS pass element. V<sub>DROP</sub> scales approximately with the output current because the PMOS device behaves as a resistor in

dropout condition.

As any linear regulator, PSRR and transient response are degraded as ( VIN – VOUT ) approaches dropout condition.

### ***OTP ( Over Temperature Protection )***

The over temperature protection function of SR8367 series will turn off the P-MOSFET when the junction temperature exceeds 160°C ( typ. ). Once the junction temperature cools down by approximately 15°C, the regulator will automatically resume operation.

### ***Thermal Application***

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T<sub>A</sub>=25°C, DSTECH PCB,

The max PD (Max)= (125°C – 25°C) / (120°C/W) = 0.83W for SOT-89-3 package.

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

$$PD = (VIN - VOUT) \times IO_{UT}$$

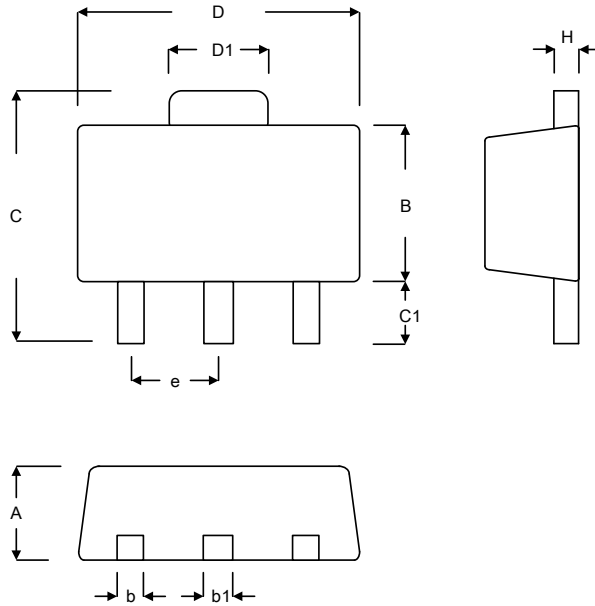
## Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the SR8367 ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.



**Package Information:**



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.397	1.600	0.055	0.063
b	0.356	0.483	0.014	0.019
B	2.388	2.591	0.094	0.102
b1	0.406	0.533	0.016	0.021
C	3.937	4.242	0.155	0.167
C1	0.787	1.194	0.031	0.047
D	4.394	4.597	0.173	0.181
D1	1.397	1.753	0.055	0.069
e	1.448	1.549	0.057	0.061
H	0.356	0.432	0.014	0.017

SOT-89-3L