High efficiency, 3A, 17V, Synchronous Step-Down Converter

1 General Description

The SR1471A/B is a synchronous step-down regulator with an internal power MOSFET. The SR1471A/B achieves 3A a of continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Hiccup protection, the cycle-by-cycle over current limit and thermal shutdown. Soft-start function reduces the stress on the input source at startup.

The SR1471A/B requires a minimal number of readily available external components, providing a compact solution.

2 Features

- Input Voltage Range: 3.5V to 17V
- Output Adjustable from 0.8V to 12V
- Low Quiescent Current: 100μA
- 150mΩ/70mΩ Low-RDS(ON) Internal Power MOSFETs.
- High efficiency operation including CCM, DCM and PSM
- 500kHz/2.2MHz switching frequency for SR1471A/B
- Internal Soft-Start
- Over-Current Protection and Hiccup
- Thermal Shutdown
- Available in a 6-pin TSOT-23 package

3 Applications

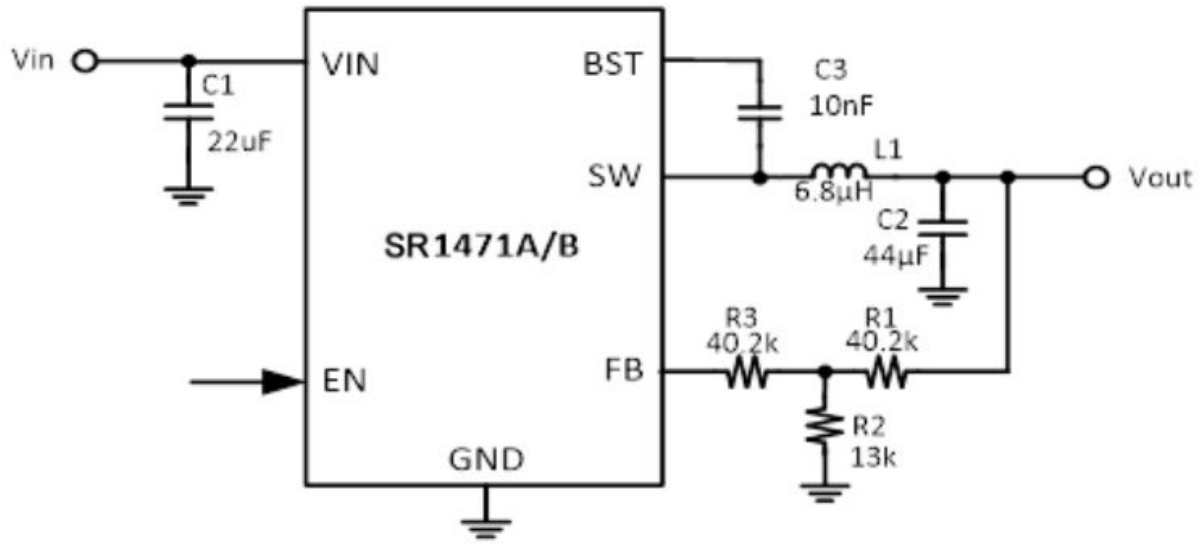
- Communication,
- Display
- Surveillance
- General Purposes

4 Ordering Information

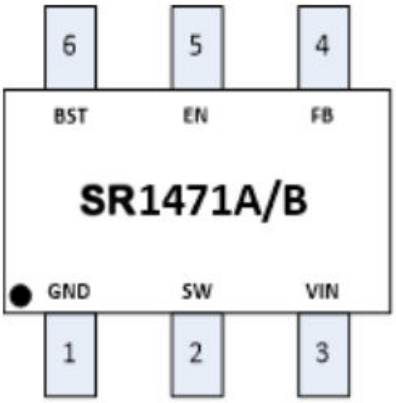
SR1471A/B
└ Package Type:
TSOT23-6P

Note:
The products are RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020 Package Information.

5 Application Circuit

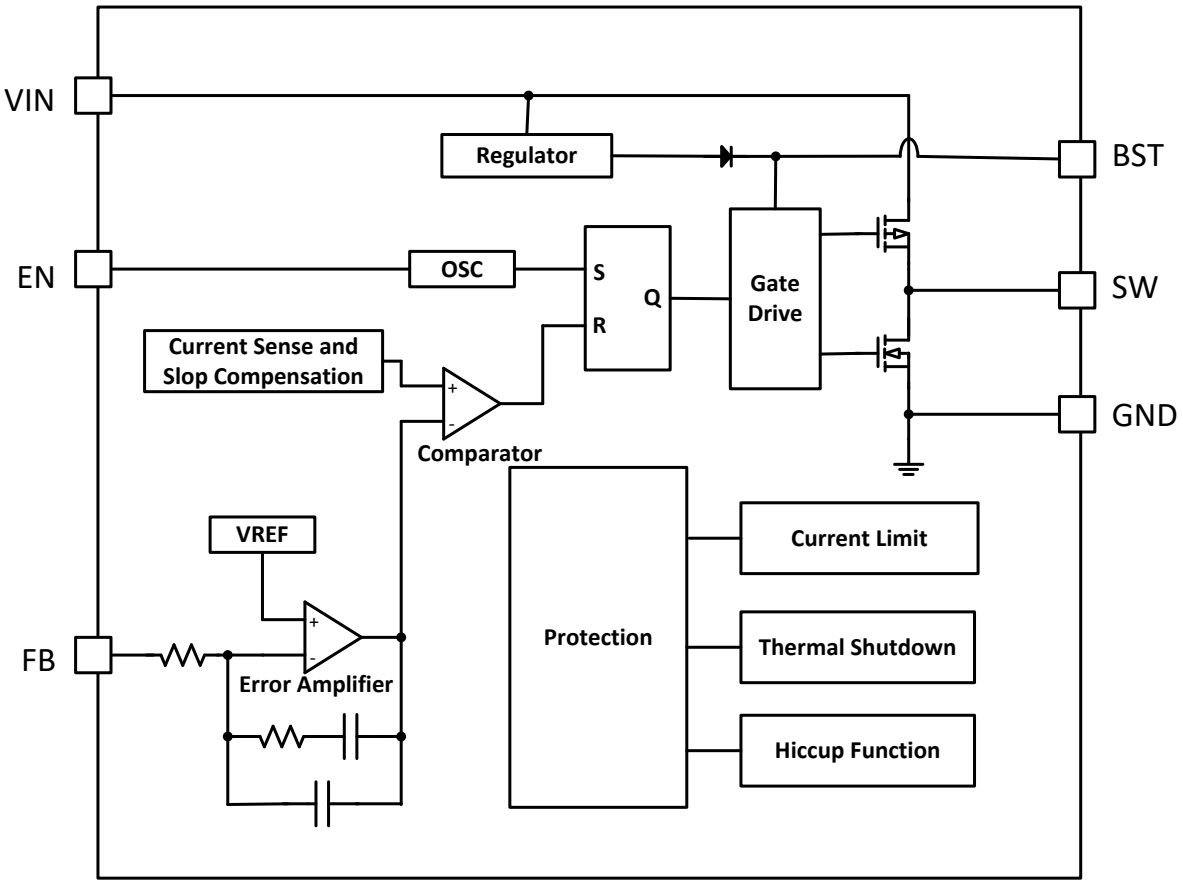


Pin Configuration and Function



Pin	Name	Function
1	GND	Power Ground.
2	SW	Switch Node. SW is the switching node that supplies power to the output.
3	VIN	Power Input. VIN supplies the power to the IC. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	FB	Feedback Input. FB senses the output voltage via an external resistive voltage divider.
5	EN	EN=HIGH to enable the BVSR1471A/B. For automatic start-up, connect EN to VIN using a 100kΩ resistor
6	BST	Bootstrap for High Side Gate Driver. Connect a 10nF capacitor from SW to BST Pin.

6 Functional Block Diagram



7 Absolute Maximum Ratings

- Supply Input Voltage: VIN to GND .....-0.3V to 19V
- Switching Voltage: SW to GND ..... -0.3V to (VIN+0.3V)
- Boot Voltage: BST to GND ..... (SW-0.3V) to (SW+6V)
- Other Pins to GND .....-0.3V to 6.0V
- Lead Temperature (Soldering, 10sec.) .....260°C
- Junction Temperature .....150°C
- Storage Temperature .....-65°C to 150°C
- ESD Susceptibility
  HBM (Human Body Model) 2KV
  MM (Machine Model) 200V

8 Recommended Operating Conditions

- Supply Input Voltage V_{IN} .....3.5V to 17V
- Junction Temperature Range.....-40°C to 125°C
- Ambient Temperature Range .....-40°C to 85°C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The device is not guaranteed to function outside its recommended operating conditions.

9 Electrical Characteristics

V_{IN}=12V, T_A=25°C, unless otherwise specified.

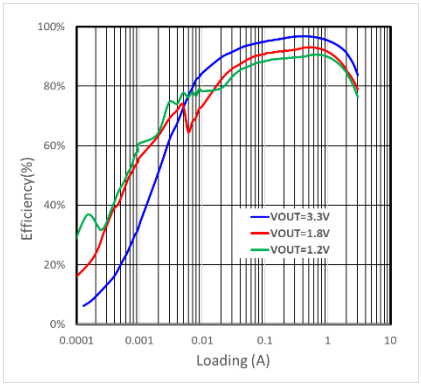
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage	V_{IN}		3.5	12	17	V
Shutdown Current	I_{SHDN}	V_{EN} = 0V measured into VIN pin. No load		0.1	1	μA
Quiescent Current	I_Q	V_{EN} = 1V and V_{FB} = 1V measured into VIN pin. No load		100		μA
Under-Voltage Lockout Threshold	V_{UVLOH}	V_{IN} Rising		3.2		V
	V_{UVLOL}	V_{IN} falling		3		V
EN Voltage	V_{IH}			1.5		V
	V_{IL}			1.2		V
HS Switch-On Resistance	$R_{DS(ON)HS}$			150		mohm
LS Switch-On Resistance	$R_{DS(ON)LS}$			70		mohm
Current Limit	I_{LIMIT}	SR1471A/B	3.5	4.2		A
Oscillator Frequency	f_{SW}	SR1471A		500		kHz
		SR1471B		2200		kHz
Maximum Duty Cycle	D_{MAX}			92		%
Minimum On Time	T_{ON_MIN}			50		nS
Feedback Voltage	V_{FB}			0.8		V
Soft-Start Period	T_{SS}			1		ms
VIN Over-Voltage	V_{OVP}			18		V
Thermal Shutdown				150		℃
Thermal Hysteresis				20		℃

10 Typical Performance Characteristics

VIN = 12V, VOUT = 3.3V, L = 6.8µH, TA = +25°C, unless otherwise specified.

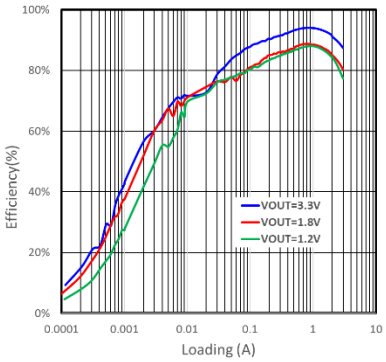
Efficiency

V_{in} = 5V, I_{OUT} = 0.001A to 3A



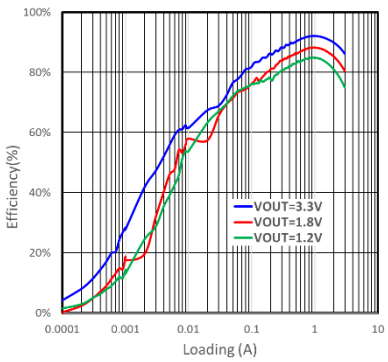
Efficiency

V_{in} = 12V, I_{OUT} = 0.001A to 3A



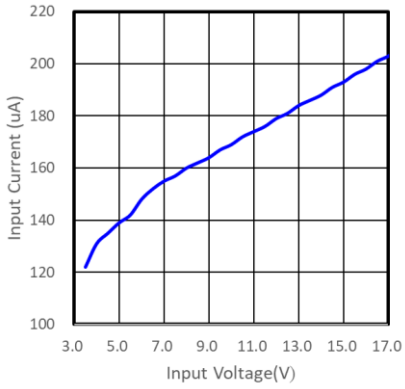
Efficiency

V_{in} = 17V, I_{OUT} = 0.001A to 3A



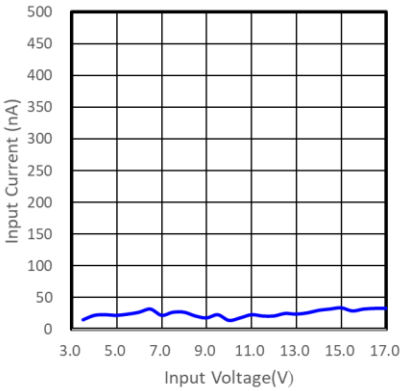
Enabled Supply Current vs. Input Voltage

V_{in} = 3.5V to 17V, I_{OUT} = 0A



Disable Supply Current vs. Input Voltage

V_{in} = 3.5V to 17V, I_{OUT} = 0A



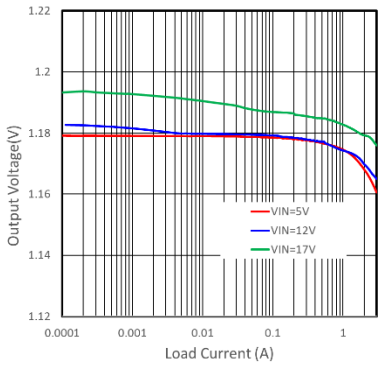
Typical Performance Characteristics *(continued)*

VIN = 12V, VOUT = 3.3V, L = 6.8µH, TA = +25°C, unless otherwise specified.

Load Regulation

V_{in} = 5V to 17 V, V_{out} = 1.2V

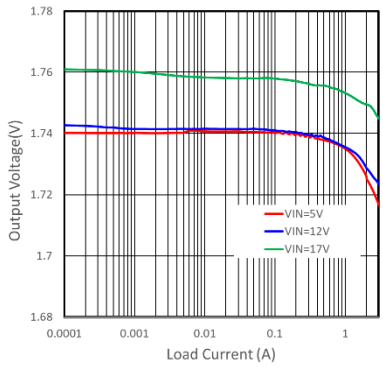
I_{OUT} = 0.001A to 3A



Load Regulation

V_{in} = 5V to 17 V, V_{out} = 1.8V

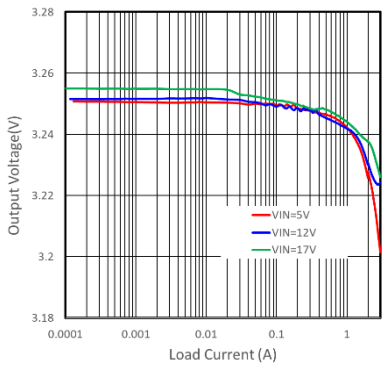
I_{OUT} = 0.001A to 3A



Load Regulation

V_{in} = 5V to 17 V, V_{out} = 3.3V

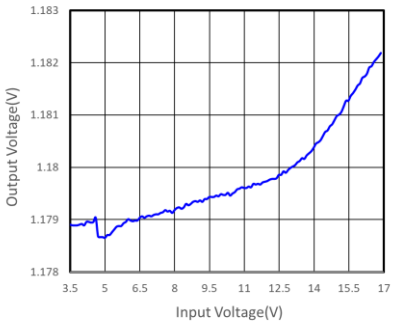
I_{OUT} = 0.001A to 3A



Line Regulation

V_{in} = 3.5V to 17V, V_{OUT} = 1.2V

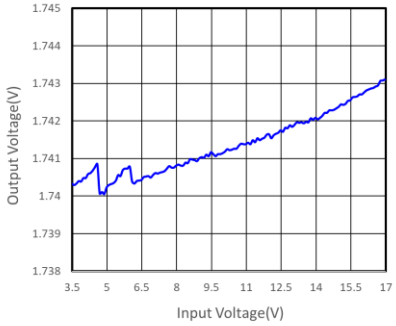
I_{OUT} = 10mA



Line Regulation

V_{in} = 3.5V to 17V, V_{OUT} = 1.8V

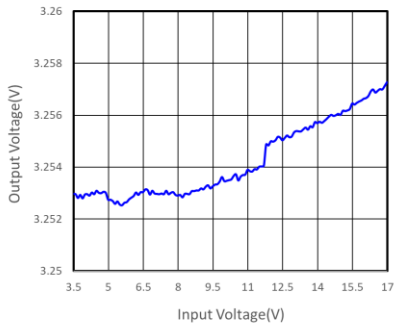
I_{OUT} = 10mA



Line Regulation

V_{in} = 3.5V to 17V, V_{OUT} = 3.3V

I_{OUT} = 10mA

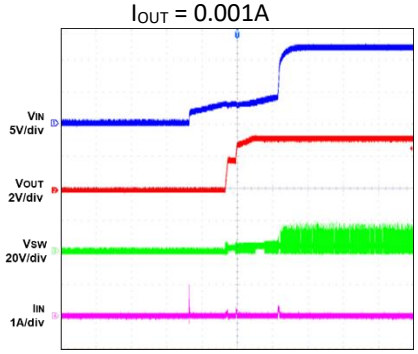


Typical Performance Characteristics *(continued)*

VIN = 12V, VOUT = 3.3V, L = 6.8µH, TA = +25°C, unless otherwise specified.

Startup through Input Voltage

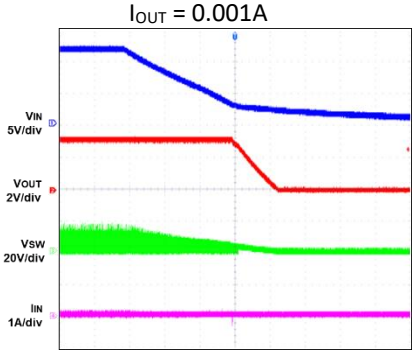
I_{OUT} = 0.001A



8ms/div

Shutdown through Input Voltage

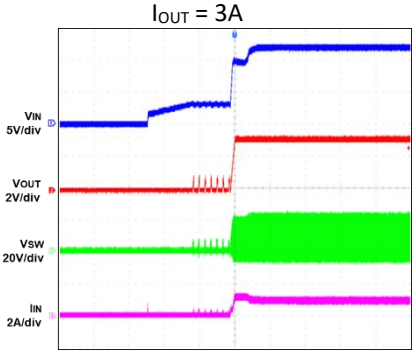
I_{OUT} = 0.001A



100ms/div

Startup through Input Voltage

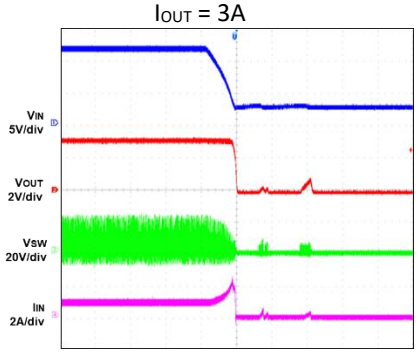
I_{OUT} = 3A



8ms/div

Shutdown through Input Voltage

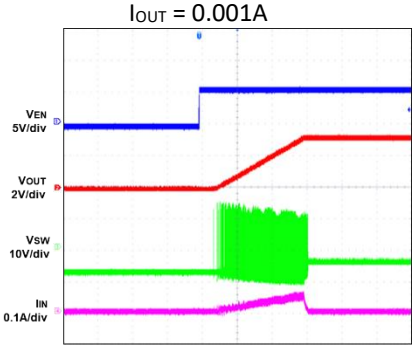
I_{OUT} = 3A



800µs/div

Startup through Enable

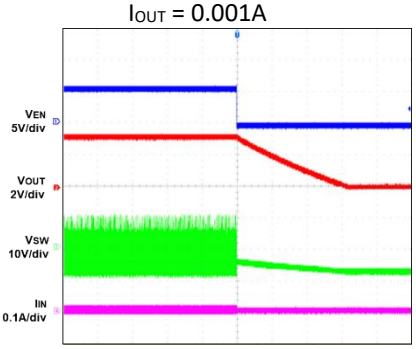
I_{OUT} = 0.001A



400µs/div

Shutdown through Enable

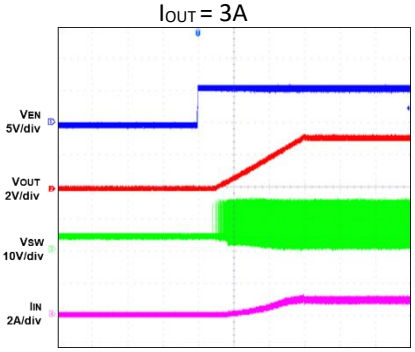
I_{OUT} = 0.001A



40ms/div

Startup through Enable

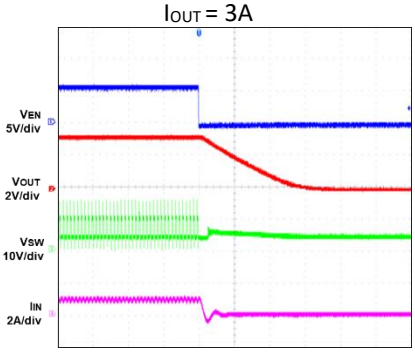
I_{OUT} = 3A



400µs/div

Shutdown through Enable

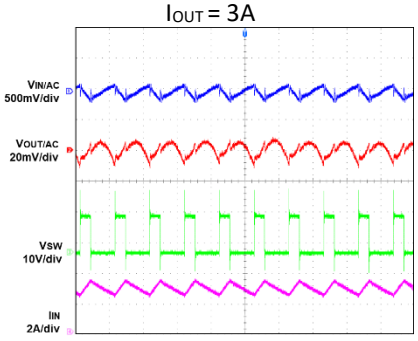
I_{OUT} = 3A



20µs/div

Input/Output Ripple

I_{OUT} = 3A



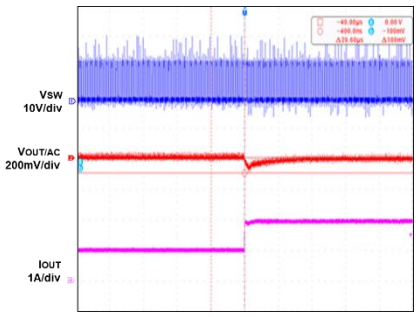
2µs/div

Typical Performance Characteristics *(continued)*

VIN = 12V, VOUT = 3.3V, L = 6.8µH, TA = +25°C, unless otherwise specified.

Transient Response

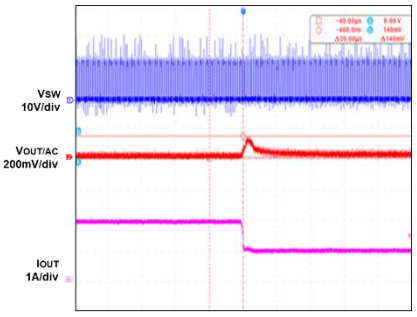
I_{OUT} = 1A to 2A



40µs /div

Transient Response

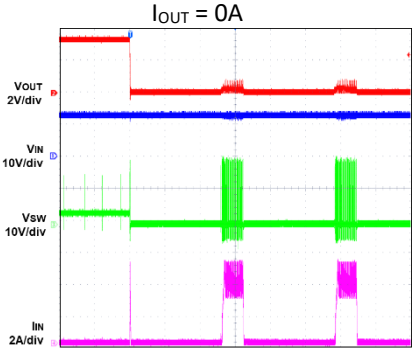
I_{OUT} = 1A to 2A



40µs /div

Short Circuit Entry

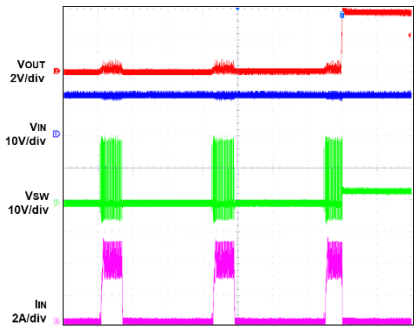
I_{OUT} = 0A



1.6ms/div

Short Circuit Recovery

I_{OUT} = 0A



1.6ms/div

11 Operation

The SR1471 is a high frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 3A peak output current over a wide input supply range, with excellent load and line regulation. The SR1471 operates in a fixed frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates the PWM cycle to turn on the integrated high-side power MOSFET. This MOSFET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the COMP set current value within 90% of one PWM period, the power MOSFET is forced to turn off.

Internal Regulator

The 5V internal regulator powers most of the internal circuits. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the regulator output is in full regulation. When V_{IN} falls below 5.0V, the output decreases.

Error Amplifier

The error amplifier compares the FB voltage against the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current charges or discharges the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control-loop design.

Enable

EN is a digital control pin that turns the regulator on and off: Drive EN HIGH to turn on the regulator, drive it LOW to turn it off.

The EN pin is clamped internally using a 5.5V series-Zener-diode as shown in Figure 1.

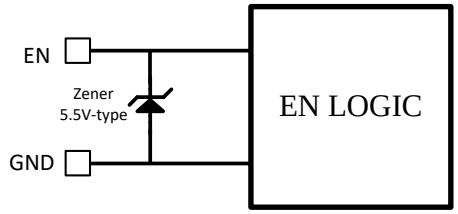


Figure 1 : 5.5V Zener Diode

Connecting the EN input pin through a pullup resistor to the V_{IN} voltage limits the EN input current to less than 100μA. For example, with 12V connected to Vin, $R_{PULLUP} \geq$ (12V-5.5V) ÷ 100μA =65kΩ). Connecting the EN pin directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ≤ 6V to prevent damage to the Zener diode.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The SR1471 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.2V while its falling threshold is consistently 3V.

Internal Soft-Start

Soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuit generates a softstart voltage (SS) that ramps up from 0V to 1.2V: When SS falls below the internal reference (REF), SS overrides REF so that the error amplifier uses SS as the reference; when SS exceeds REF, the error amplifier resumes using REF as its reference. The SS time is internally set to 1ms.

Over-Current-Protection and Hiccup

The SR1471 has a cycle-by-cycle over-current limit for when the inductor current peak value exceeds the set current-limit threshold. First, when the output voltage drops until FB falls below the Under-Voltage (UV) threshold (typically 0.15V) to trigger a UV event, the SR1471 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current to alleviate thermal issues and to protect the regulator. The SR1471 exits hiccup mode once the overcurrent condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C) the chip is enabled again.

Driver and Bootstrap Charging

An external bootstrap capacitor powers the power MOSFET driver. This driver has its own UVLO protection, with a rising threshold of 2.2V. VIN regulates the bootstrap capacitor voltage internally through D1, M1, R4, C4, L1 and C2 (Figure 2). If (VIN-VSW) exceeds 4.5V, U2 will regulate M1 to maintain a 5V BST voltage across C4.

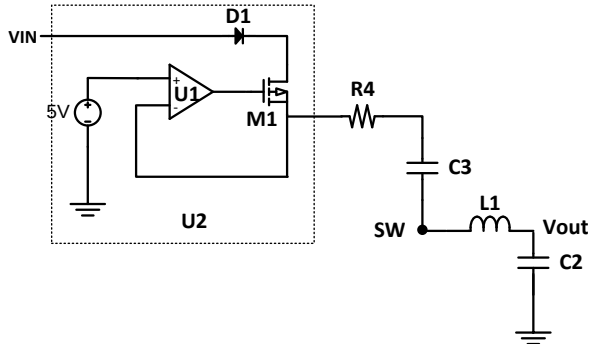


Figure 2 : Internal Bootstrap Charging Start-Up and Shutdown Circuit

If both VIN and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.Three events can shut down the chip: EN low, VIN low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The driver is not subject to this shutdown command.

12 Application Information

Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistor R1 also sets the feedback-loop bandwidth through the internal compensation capacitor (see the Typical Application circuit). Choose R1 around 10kΩ, and R2 by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Use a T-type network for when V_{OUT} is low.

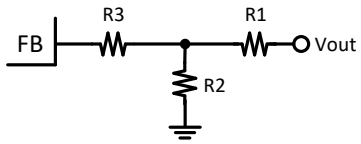


Figure 3: T-Type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1—Resistor Selection for Common Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	LOUT (uH)	COUT (uF)
1.2	20.5	41.2	120	2.2	44
1.8	40.2	32.4	75	3.3	44
3.3	40.2	13	40.2	6.8	44

Selecting the Inductor

Use a 1µH-to-10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{osc}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductance for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. Use low ESR capacitors for the best performance, such as ceramic capacitors with X5R or X7R dielectrics of their low ESR and small temperature coefficients. A 22µF capacitor is sufficient for most applications. The input capacitor (C1) requires an adequate ripple current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at V_{IN} = $2V_{OUT}$, where :

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. Place a small, high-quality, ceramic capacitor (0.1µF) as close to the IC as possible when using electrolytic or tantalum capacitors. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C_1} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_s \times C_2})$$

Where L_1 is the inductor value and RESR is the equivalent series resistance (ESR) of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The SR1471 can be optimized for a wide range of capacitance and ESR values.

13 Layout Guidelines

For the best performance of the SR1471 , the basic principles listed should be strictly followed and Figure 5 as reference.

- Place C1 as close as possible to the BST and SW pins respectively
- Place C5 and C6 as close as possible to the VIN pins respectively
- Place L1 as close as possible to the SW pins
- PCB layout of SW pins should be far away from sensitive analog areas such as FB
- For good regulation, the power traces should be wide and short especially for the high current output loop

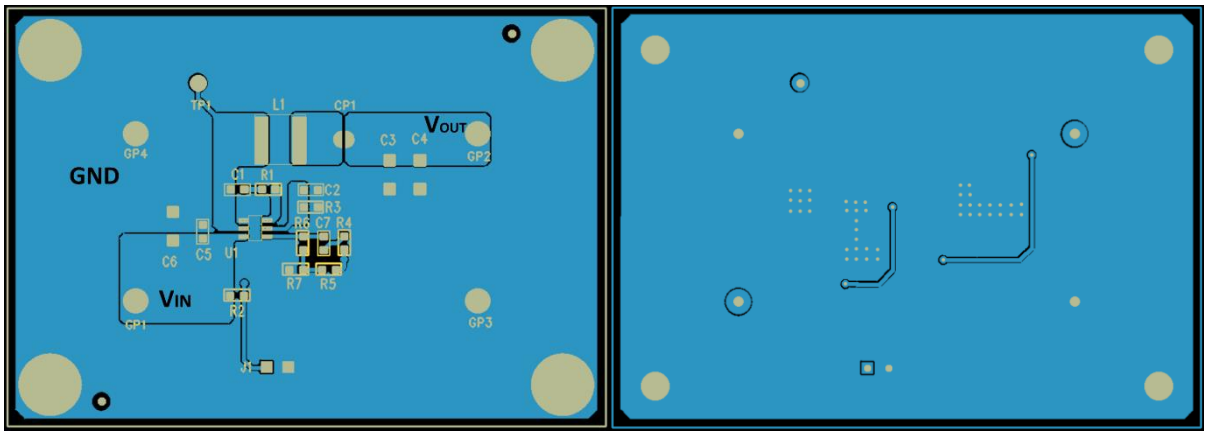
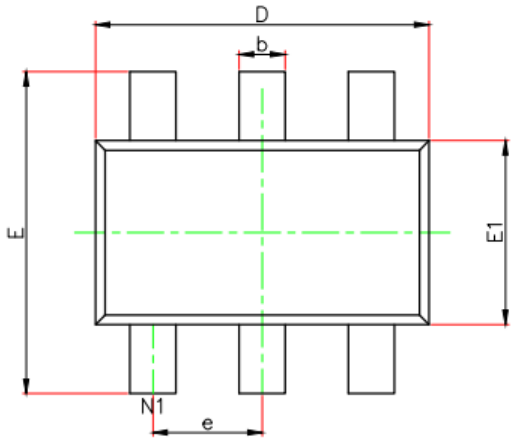


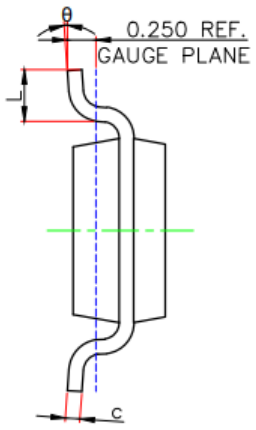
Figure 5: Sample Layout

14 Package Information

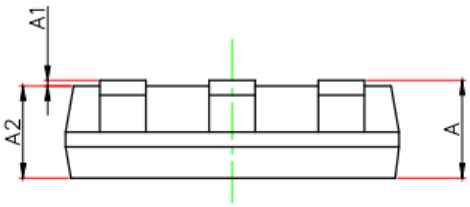
TSOT-23-6L(16R)(FC) PACKAGE OUTLINE DIMENSIONS



TOP VIEW



SIDE VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	------	1.100	-------	0.043
A1	0.000	0.100	0.000	0.004
A2	0.700	1.000	0.028	0.039
D	2.850	2.950	0.112	0.116
E	2.650	2.950	0.104	0.116
E1	1.550	1.650	0.061	0.065
b	0.300	0.500	0.012	0.020
c	0.080	0.200	0.003	0.008
e	0.950(BSC)		0.037(BSC)	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°