Wide Input Range 3.8V to 36V, 2A Synchronous Step-Down Converter

1 General Description

The SR33620 is a synchronous step-down converter integrated high-side and low-side power MOSFETs and achieves output current of 3A with wide input voltage range from 3.8V to 36V. The tolerance of input voltage goes up to 38V which can reduce the necessary design effort to protect against over-voltages.

The SR33620 uses peak-current-mode control to achieve optimal efficiency and increase accuracy of output voltage. It has selectable switching frequency which can operate with 400kHz, 1.4MHz or 2.1MHz. Load transient performance is improved with Forced-PWM feature in the corresponding frequency regulator. The high precision of enable pin gives flexibility by enabling a direct connection to the wide input voltage or precise control over device start-up and shutdown. The power-good flag offers a true signal of system status in time eliminating the requirement for an external circuit.

2 Features

- Wide Input Voltage Range: 3.8V to 36V
- Output voltage range: 1V to 24V
- Maximum Output Current: 2A
- 400kHz/1.4MHz/2.1MHz frequency options for A/B/C
- Auto PFM/PWM options
- Increased light load efficiency in PFM
- Low operating quiescent current of 40 μA

3 Applications

- Automotive System

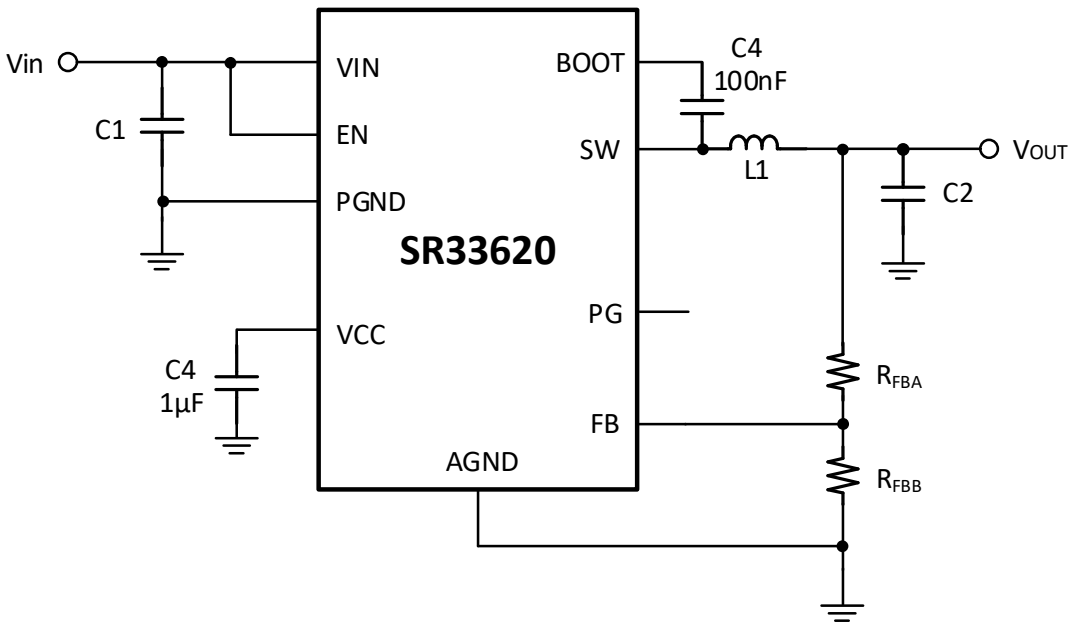
4 Device Information

Part Number	Package	Body Size
SR33620FWQ	FCQFN(12)	2.0mm x 3.0mm
SR33620SOP	SOP(8)	3.9mm x 4.9mm

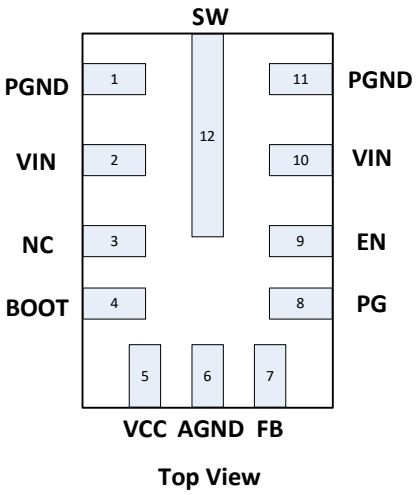
(1) For all available package, see the orderable addendum at the end of the datasheet.

Note:
The products are RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020Package Information.

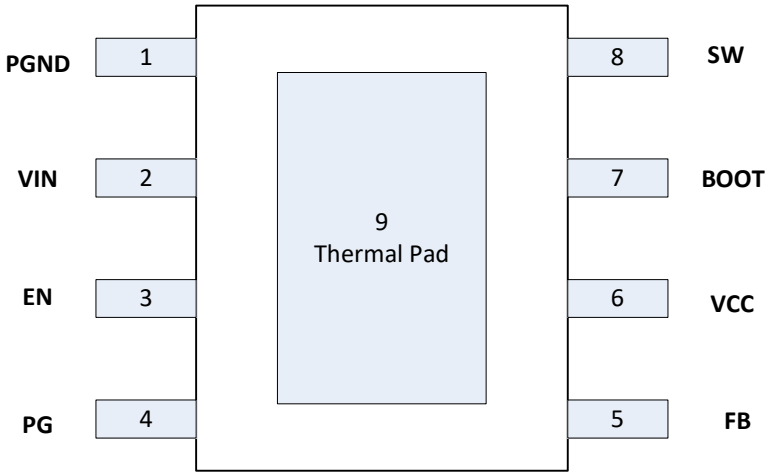
5 Application Circuit



6 Pin Configuration and Function



Top View



Top View

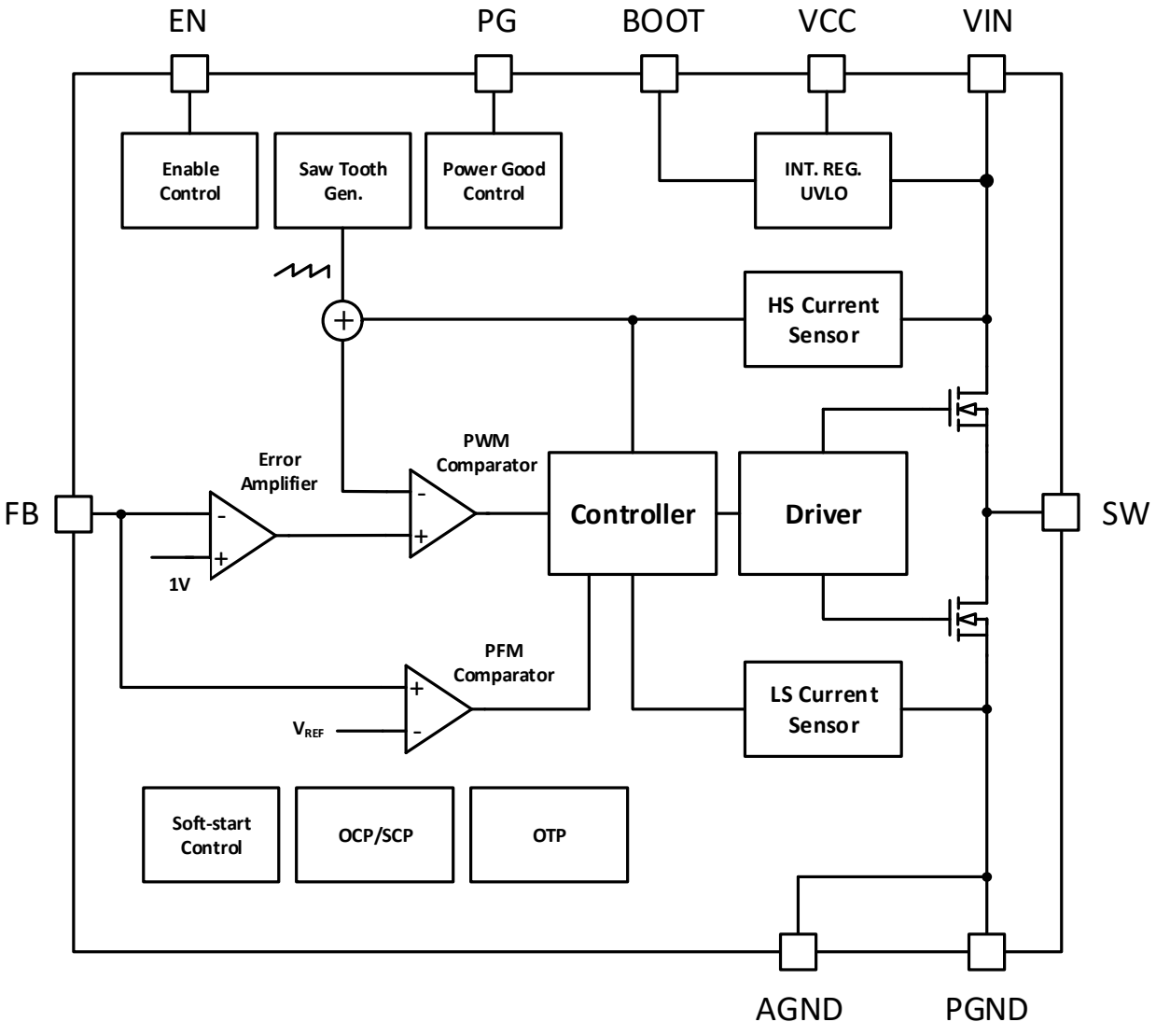
QFN12L Pin	SOP8L Pin	Name	Function
1, 11	1	PGND	Power Ground.
2, 10	2	VIN	Power input for SR33620
3	-	NC	The NC pin has no connection to internal regulator. It is recommended to connect with the SW pin on the PCB to simplify the layout of BOOT capacitor.
4	7	BOOT	Bootstrap for High Side Gate Driver. Connect a 100nF capacitor from SW to BOOT Pin.
5	6	VCC	VCC pin is an internal 5V LDO output. Used as supply to internal control circuits. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND. Note that this pin cannot connect to external loads.
6	9	AGND	Analog Ground.
7	5	FB	Feedback Input. FB senses the output voltage via external resistive voltage divider. Note that this pin cannot float or connect to GND.
8	4	PG	Power-good flag output connect to suitable voltage supply through a current limiting resistor. In high level, it means power OK. Otherwise, it means power bad in low level. Goes low when EN = Low. Can be open or grounded when not used.
9	3	EN	EN pin enables or disables SR33620. A high level turns on and a low level turns off.
12	8	SW	Switch pin is the switching node that supplies power to the output. Connect the inductor to this terminal. It is recommended to connect with the NC pin on the PCB to simplify the layout of BOOT capacitor.

7 Device Comparable Table

Device Option	Package	Frequency	Forced-PWM	Rated Current
SR33620FWQA00	FWQ Flip Chip QFN 12L 2.0mm x 3.0mm	400kHz	N	2A
SR33620FWQB00		1.4MHz	N	
SR33620FWQC00		2.1MHz	N	
SR33620SOPA00	SOP SOP 8L 3.9mm x 4.9mm	400kHz	N	2A
SR33620SOPB00		1.4MHz	N	
SR33620SOPC00		2.1MHz	N	
SR33620FWQAF00	FWQ Flip Chip QFN 12L 2.0mm x 3.0mm	400kHz	Y	2A
SR33620FWQBF00		1.4MHz	Y	
SR33620FWQCF00		2.1MHz	Y	
SR33620SOPAF00	SOP SOP 8L 3.9mm x 4.9mm	400kHz	Y	2A
SR33620SOPBF00		1.4MHz	Y	
SR33620SOPCF00		2.1MHz	Y	

Note: XX (00-99) is the customer code setting by the built-in NVM for output voltage, power sequence and register setting.

8 Functional Block Diagram



9 Absolute Maximum Ratings

- Supply Input Voltage: VIN to PGND .....-0.3V to 38V
- Switching Voltage: SW to PGND ..... -0.3V to (VIN+0.3V)
- Enable Voltage: EN to AGND ..... -0.3V to (VIN+0.3V)
- Power Good Flag: PG to AGND .....-0.3V to 22V
- Other Pins (FB, VCC) to AGND .....-0.3V to 5.5V
- BOOT to SW .....-0.3V to 5.5V
- AGND to PGND .....-0.3V to 0.3V
- Power Dissipation, PD@ TA=25°C
  QFN12L..... 1.5W
  SOP8L..... 1.667W
- Package Thermal Resistance
  QFN12L..... 66.65°C/W
  SOP8L..... 60°C/W
- Lead Temperature (Soldering, 10sec.) 260
- Junction Temperature .....-40°C to 150°C
- Storage Temperature .....-65°C to 150°C
- ESD Susceptibility
  HBM (Human Body Model) 2.5KV
  CDM (Charged Device Model)..... 750V

10 Recommended Operating Conditions

- Supply Input Voltage .....3.8V to 36V
- Enable Voltage[3].....0V to 36V
- PG Voltage[3] .....0V to 18V
- Junction Temperature Range.....-40°C to 125°C
- Ambient Temperature Range .....-40°C to 85°C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

   The device is not guaranteed to function outside its recommended operating conditions.

   The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.

11 Electrical Characteristics

V_{IN}=12V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Input						
Input Supply Voltage	V_{IN}		3.8	12	36	V
VIN Undervoltage Lockout	V_{IN_UVLOH}	VIN Rising	3.6	3.7	3.8	V
	V_{IN_UVLOL}	VIN Falling	3.1	3.3	3.5	V
Quiescent Current	I_Q	Non-switching input current; measured into VIN pin. FB=1.2V		40		μA
Shutdown Current	I_{SHDN}	EN=0V measured into VIN pin. No load		10		μA
Power Stage						
HS Switch-On Resistance	$R_{DS(ON)\_HS}$	QFN12L		75	145	mΩ
LS Switch-On Resistance	$R_{DS(ON)\_LS}$	QFN12L		50	95	mΩ
HS Switch-On Resistance	$R_{DS(ON)\_HS}$	SOP8L		95	160	mΩ
LS Switch-On Resistance	$R_{DS(ON)\_LS}$	SOP8L		65	110	mΩ
Oscillator Frequency	f_{SW}	400 kHz	340	400	460	kHz
	f_{SW}	1.4 MHz	1.2	1.4	1.6	MHz
	f_{SW}	2.1 MHz	1.95	2.1	2.35	MHz
Maximum Switch Duty Cycle	D_{MAX}			98		%
Maximum Switch On-time	t_{ON_MAX}			7	12	μs
Minimum Switch On-time	t_{ON_MIN}			55	83	ns
Minimum Switch Off-time	t_{OFF_MIN}			53	73	ns
Internal Soft-start Time	t_{SS}		3	4.5	6	ms
Switch Voltage Dead Time	t_D			2		ns
Enable (EN)						
EN pin high level for V_{CC} start up	$V_{EN\_VCC\_H}$	V_{ENABLE} rising			1.14	V
EN pin low level for V_{CC} shutdown	$V_{EN\_VCC\_L}$	V_{ENABLE} falling	0.3			V
EN pin high level for V_{OUT} start up	$V_{EN\_VOUT\_H}$	V_{ENABLE} rising	1.157	1.231	1.3	V
EN pin hysteresis for V_{OUT} shutdown	$V_{EN\_VOUT\_HYS}$	Hysteresis below $V_{ENABLE-H}$ falling		110		mV
EN pin leakage current	I_{EN_LEAK}	V_{EN} = 3.3V		0.2		nA
Internal 5V LDO (VCC)						
Internal VCC Voltage	V_{CC}	6V ≤ V_{IN} ≤ 36V	4.75	5	5.25	V
Voltage Reference (FB)						
Feedback Voltage	V_{FB}		0.985	1	1.015	V
Feedback Leakage Current	I_{FB_LEAK}	FB = 1V		0.2		nA
Hiccup Mode Trip Voltage	V_{HC}	FB pin voltage required to trip short-circuit hiccup mode.		0.4		V
Hiccup Burst Interval Time	t_{HC}	Time between current-limit hiccup burst		94		ms

Electrical Characteristics (Continued)

V_{IN}=12V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Good (PG)						
Power-Good Upper Threshold	V_{PGTHH}	Power-Good Voltage Rising (% of FB voltage)	105	107	110	%
Power-Good Lower Threshold	V_{PGTHL}	Power-Good Voltage Falling (% of FB voltage)	90	93	95	%
Power-Good hysteresis (rising & falling)	V_{PG_HYS}	% of FB voltage		2		%
Power-Good rising/falling edge deglitch delay	t_{PG}		80	140	200	μs
Minimum input voltage for proper Power-Good function	$V_{PG-VALID}$				2	V
Power-Good on-resistance	R_{PG}	V_{EN} = 2.5V		50	190	mΩ
Protection						
High-side MOSFET Current Limit	I_{HS_LIMIT}		2.9	3.5	4	A
Low-side MOSFET Current Limit	I_{LS_LIMIT}		1.95	2.45	2.9	A
Zero cross detector threshold	I_{ZCTH}	PFM variants only		-0.1		A
Minimum inductor peak current	I_{LPEAK_MIN}	V_{OUT}=5V		0.4		A
Thermal Shutdown	T_{SHDN}			170		℃
Thermal Hysteresis				20		℃

12 Operation

Enable and Shutdown (EN)

Start-up and shutdown are controlled by the EN pin which features precision thresholds. An external voltage divider can be used to provide an adjustable UVLO input. When the EN voltage is higher than $V_{EN-VCC-H}$, the BVP SR33620 will enter standby mode and power the internal VCC. Increasing the EN voltage to $V_{EN-OUT-H}$ fully enables the device, allowing it to start the soft-start period and produce output voltage. When the EN voltage is below $V_{EN-OUT-H}$ by $V_{EN-OUT-HYS}$, the regulator stops running and enters standby mode. As EN voltage further decreases below $V_{EN-VCC-L}$, the device completely shuts down. Enable function behavior is shown in Figure 1. The EN input can be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in *Electrical Characteristics*.

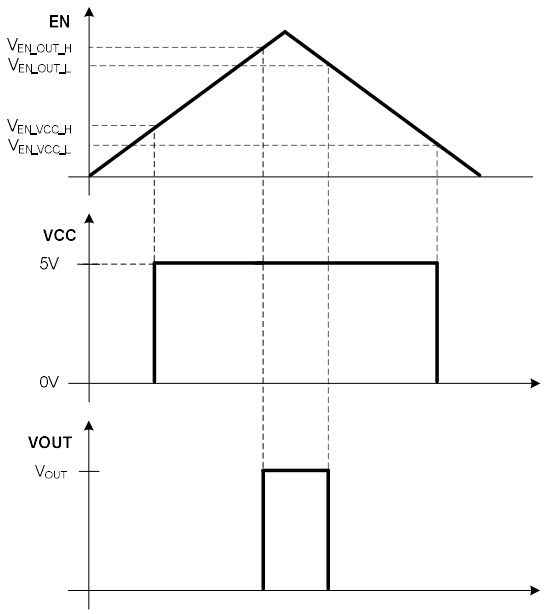


Figure 1. Enable Function Behavior

Under-Voltage Lockout (UVLO)

The SR33620 integrates an undervoltage-lockout feature in the VIN pin. When VIN reaches 3.7V, the device receives the EN signal and starts switching. As VIN falls below 3.3V, device shuts down regardless of EN status. Because the LDO is in dropout during these transitions, the previously mentioned values roughly represent the input voltage levels during the transitions.

Over Current and Short Circuit Protection

The SR33620 integrates valley current limit and peak current limit for overloads and short-circuits protection. Peak current limit is used to protect the high-side power MOSFET from excessive current. When hiccup mode is used for short circuits, cycle-by-cycle current limit is used for overloads. Finally, a zero current detector is used on the low-side power MOSFET to implement diode emulation mode (DEM) at light loads. During overloads, the low-side current limit, I_{LS_LIMIT}, determines the maximum load current that the SR33620 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not reduce below I_{LS_LIMIT} before the next turn on cycle, then that cycle is skipped. The low-side MOSFET will keep on until the current reduces below I_{LS_LIMIT}. The maximum load current can calculate with formula shown in Equation 1.

$$I_{OUT\_max} = I_{LS\_LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \times f_{sw} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where

- f_{SW}: Switching frequency
- L : Inductance

When the voltage of FB input is under 0.4V due to a short circuit during current limit, the device will enter hiccup mode. In this mode, the device stops switching for t_{HC} which is about 94 ms and then restart with soft start. If the status remains short circuit after restart, the device runs in current limit for about 20 ms and shuts down again. This cycle will repeat until the status of short circuit has been removed. This mode can help to reduce the output current substantially and prevent the temperature rise rapidly of the device. The short-circuit transient and recovery as shown in figure 2. The high-side-current limit trips when the peak inductor current reaches I_{HS_LIMIT}. This is a cycle-by-cycle current limit and does not produce any frequency or load current foldback. The purpose is to protect the high-side MOSFET from excessive current. If this current limit trips before the low-side protection, such as high input voltages, I_{HS_LIMIT} determines the maximum output current. Note that I_{HS_LIMIT} varies with duty cycle.

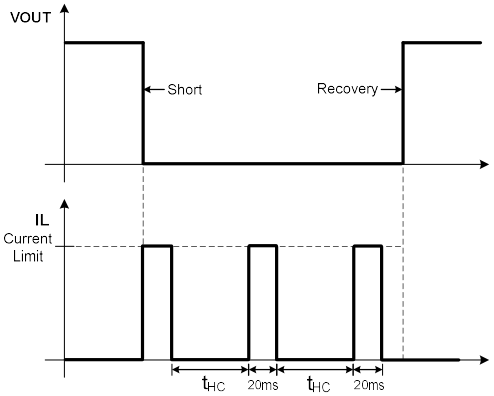


Figure 2. Short-Circuit Transient and Recovery

Power-Good Flag Output

When output voltage is out of regulation, the power-good flag function (PG pin) of the SR33620 can be used to reset a system microprocessor. The PG flag output goes low when the device is under fault conditions, such as current limit and thermal shutdown, or during normal start-up. False flag operation will be prevented by glitch filter for short excursions of the output voltage, such as during line and load transients. If the output voltage excursions continue less than t_{PG}, the power-good flag will not trip. Power-good operation described as above is shown in Figure 3 and Figure 4. Note that during initial power-up, a delay of about 4ms is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function. The power-good output can also be pulled up to either VCC or VOUT through an appropriate resistor as desired. If this function is not needed, the PG pin must be grounded. When EN is pulled low, the flag output is also forced low.

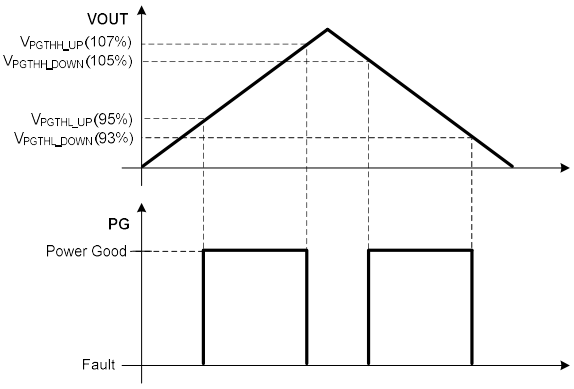


Figure 3. Power-Good Operation

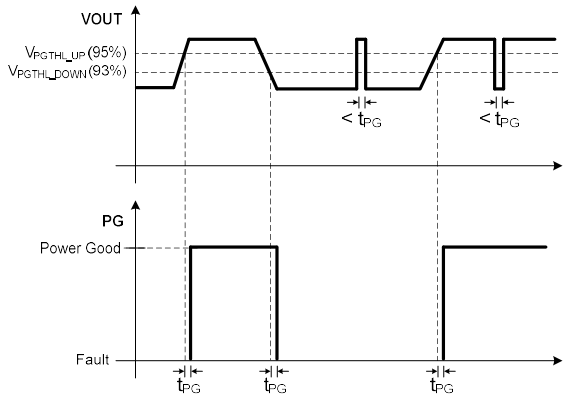


Figure 4. Power-Good Timing Behavior

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. When the junction temperature exceeds 170°C, it shuts down the whole device. When the junction temperature falls below its lower threshold (typically 150°C), the device restart.

The PFM/PWM Mode

In this mode, the device will operate with PFM or PWM as load changes. At light load, the device operates in PFM (Pulse Frequency Modulation). In this mode, the high-side MOSFET is turned on to generate a burst of one or more pulses to provide power to the load. The duration of the burst depends on when the inductor current reaches $I_{LPEAK-MIN}$. The frequency of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency. This mode provides high efficiency in light load by reducing the amount of input current, but it also causes larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depend on the input voltage, output voltage, and load.

At medium and high load conditions, the device enters PWM (Pulse Width Modulation) mode automatically and operates in a constant switching frequency (f_{SW}). While operating in PWM mode, the output voltage is regulated by modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

The Forced PWM Mode

In Forced PWM operation, the diode emulation feature is turned off. The device operates with a constant switching frequency all over the load range. Under some conditions where the device

must reduce the on-time or off-time below the ensured minimum value to maintain regulation, the frequency reduces to maintain the effective duty cycle required for regulation. This occurs for very high and very low input/output voltage ratios. In Forced PWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the output of the regulator to its input. Note that in Forced PWM mode, larger currents pass through the inductor. If the device is in light load, PFM/PWM mode is better than forced PWM mode. Once loads are heavy enough to necessitate CCM operation, forced PWM mode has no measurable effect on regulator operation.

13 Application Information

Selecting the Inductor

The inductor value affects the peak-to-peak ripple current, PWM-to-PFM transition point, output voltage ripple and efficiency. For most designs, derive the inductance value from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current. Choose an inductor ripple current is approximately 30% of the maximum load current. Choose inductor must consider DC resistance and saturation current. The saturation current rating of the inductor is at least as large as the high side switch current limit, I
This ensures that the inductor does not saturate even during a short circuit on the output. For high efficiency, an inductor with a DC resistance should be selected as low as possible.

Table 1. Components Suggestion

V_{OUT} (V)	f_{SW} (kHz)	L1 (uH)	C1 (uF)	C2 (uF)
3.3	400	6.8	10+0.2 or similar	4 x 22
	1400	2.2		2 x 22
	2100	1.2		2 x 22
5.0	400	8		4 x 22
	1400	2.2		2 x 22
	2100	1.5		2 x 22
12	400	15		4 x 22
	1400	4.7		4 x 10
	2100	3.3		4 x 10

Minimum Switch On-Time

To help extend the minimum controllable duty cycle, the SR33620 automatically reduces the switching frequency when the minimum on-time limit is reached. An estimate for the approximate input voltage, for a given output voltage, before frequency foldback occurs, is found in Equation as below. As the input voltage is increased, the switch on-time (duty cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \times f_{SW}}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. Use low ESR capacitors for the best performance, such as ceramic capacitors with X5R or X7R dielectrics of their low ESR and small temperature coefficients. A 10µF input capacitor is sufficient for most applications. The input capacitor (C1) requires an adequate ripple current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.
The input capacitor can be electrolytic, tantalum, or ceramic. Place a small, high-quality, ceramic capacitor (0.1µF) as close to the IC as possible when using electrolytic or tantalum capacitors.
When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C_1} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Setting the Output Voltage

The output voltage of SR33620 is externally adjustable using a resistor divider circuit. The divider network is comprised of R_{FBA} and R_{FBB} which must close the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a trade-off between excessive noise pickup and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBA} is 100 kΩ; with a maximum value of 1 MΩ. If a 1 MΩ is selected for R_{FBA}, then a feedforward capacitor must be used across this resistor to provide adequate loop phase margin. Once R_{FBA} is selected, Equation is shown as below used to select R_{FBB}. V_{REF} is nominally 1 V.

$$R_{FBB} = \frac{R_{FBA}}{\frac{V_{OUT}}{V_{REF}} - 1}$$

Table 2. Feedback Resistor selection

V_{OUT} (V)	R_{FBA} (kΩ)	R_{FBB} (kΩ)
3.3	100	43.2
5.0	100	24.9
12	100	9.09

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output

$$\frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_s \times C_2})$$

is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor. The characteristics of the output capacitor also affect the stability of the regulation system.

Bootstrap Capacitor

The SR33620 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1μF and 16V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function. A value in the range of 10kΩ to 100kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V.

External UVLO

The SR33620 can achieve external UVLO by using the circuit shown in Figure 5. The input voltage at which the device turns on is designated V_{ON} and the turnoff voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ and then Equation below is used to calculate R_{ENA} and V_{OFF}.

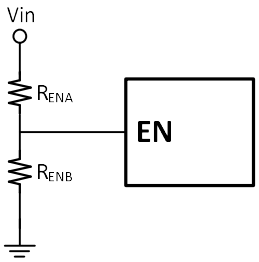


Figure 5. External UVLO Circuit

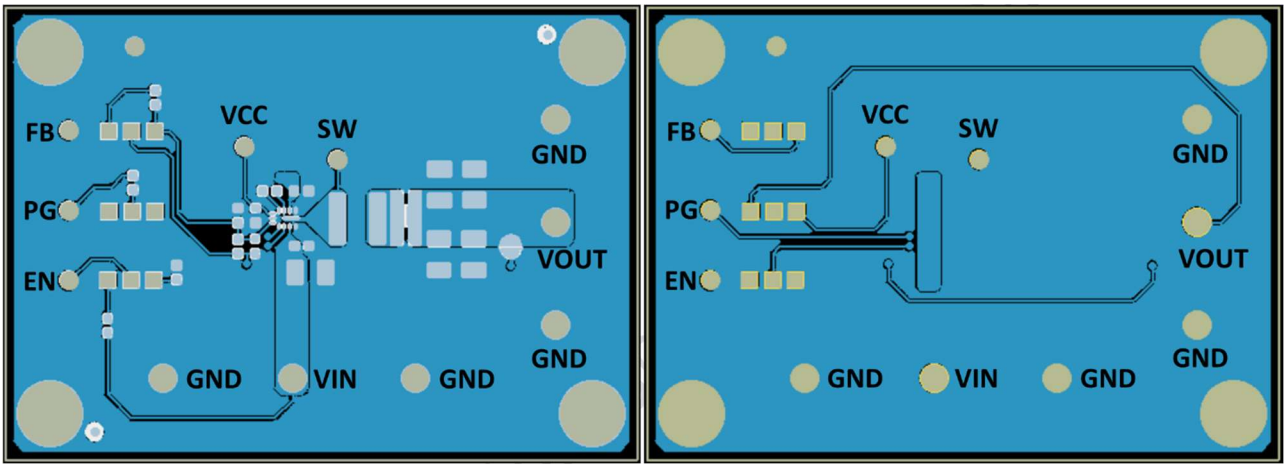
$$R_{ENA} = (\frac{V_{ON}}{V_{EN\_OUT\_H}} - 1) \times R_{ENB}$$

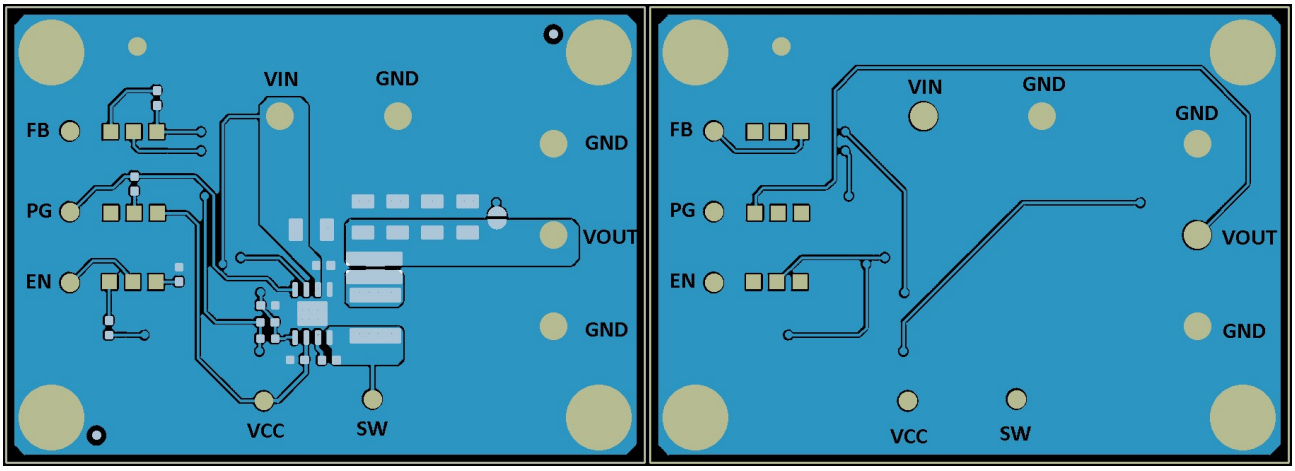
$$V_{OFF} = (1 - \frac{V_{EN\_HYS}}{V_{EN}}) \times V_{ON}$$

14 Layout Guidelines

For the best performance of the SR33620, the basic principles listed should be strictly followed. Figure 6/7 as reference for different packages.

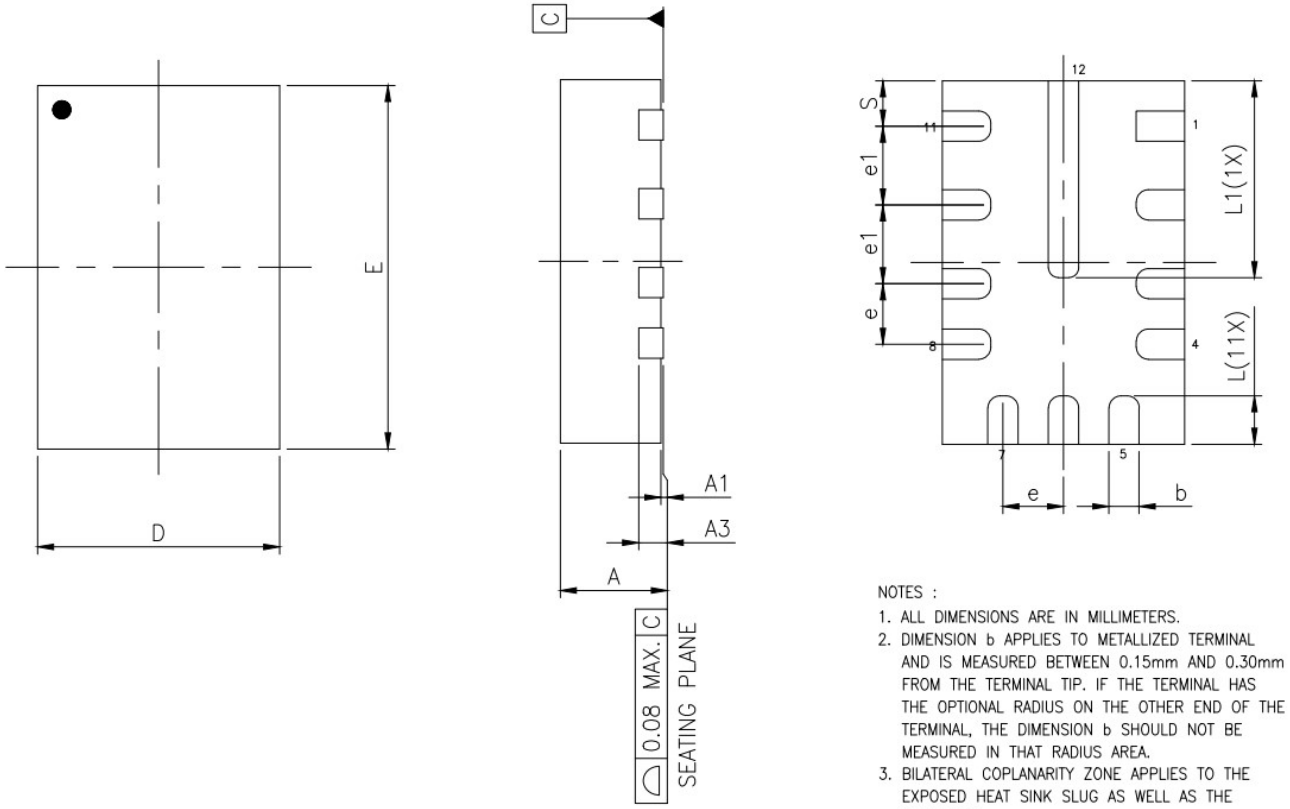
- Place input capacitor as close as possible to the VIN and GND pins respectively
- Place bypass capacitor for VCC as close as possible to the VCC and GND pin.
- Place C_{BOOT} capacitor as close as possible to the BOOT and SW pin. Route the SW pin to the N/C pin and use this path to connect the BOOT capacitor to SW. The traces must be short and wide.
- Place the feedback divider as close as possible to the FB pin. The connections to FB and GND must be short and close to those pins on the device.
- PCB layout of SW pins should be far away from sensitive analog areas such as FB.
- Place inductor as close as possible to the SW pins
- For good regulation, the power traces should be wide and short especially for the high current output loop.





15 Package Information

- **QFN12L**

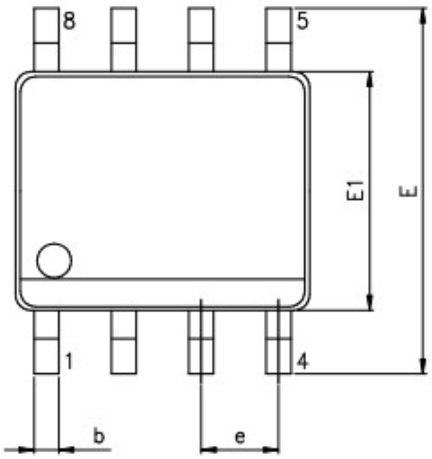


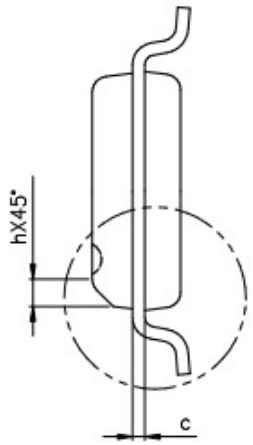
NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

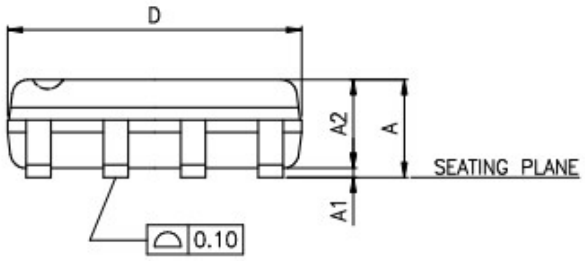
JEDEC OUTLINE	N/A		
PKG CODE	VQFN		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	1.90	2.00	2.10
E	2.90	3.00	3.10
e	0.50 BSC		
e1	0.65 BSC		
L	0.35	0.40	0.45
L1	1.575	1.625	1.675
S	0.375 REF.		

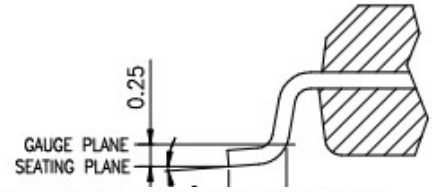
PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

- **SOP8L**



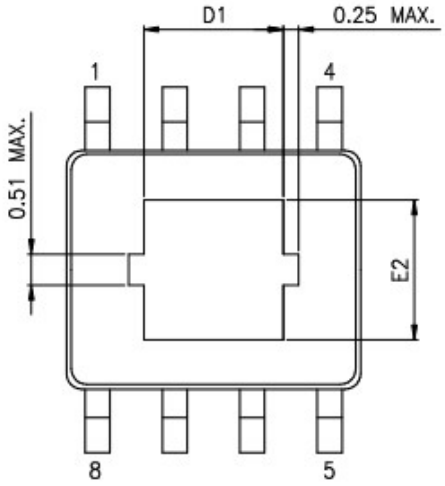






VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	STANDARD		THERMAL	
	MIN.	MAX.	MIN.	MAX.
A	—	1.75	—	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	—	1.25	—
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	4.90 BSC		4.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8



THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D1		D2	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
95*X15*	1.83	2.56	3.02	3.96	—	—

16 VERSION HISTORY

Version #	Implemented By	Revision Date	Approved By	Reason
0.1	Sming	08/09/2021		Initial Design Definition draft
0.2	Sming	Mar, 2022		1.Add SOP8 relevant information. 2.Modify ordering information. 3. Add Device Comparable Table. 4.Modify Electrical Characteristics. 5.Modify layout Guidelines. 6.Add Outline Dimension.